Finite Fourier transform distance protection for e.h.v. transmission systems.

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FINITE FOURIER TRANSFORM DISTANCE PROTECTION FOR E.H.V. TRANSMISSION SYSTEMS

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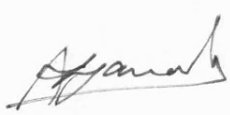

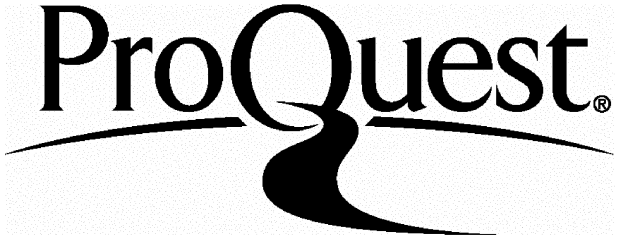

This Thesis is dedicated to my Parents

SUMMARY

This thesis describes the development of a new distance protection relay for the protection of extra high voltage (e.h.v.) transmission lines.

The new algorithm developed is based on relating the Fourier Transform of a finite window of information to the first order transmission line model measurands of the fault loop impedance. This algorithm is implemented using a discrete signal processing technique. In this technique samples of voltage and current are fed to the relay.

The algorithm is tested using a conventional hardware structure. This structure consists of a data acquisition unit, a microcomputer and a multiplier unit incorporating a fast hardware multiplier. For the process implementation, a quadrilateral characteristic is used and a trip signal is initiated when the measurands converge to this region. In order to maintain the speed-accuracy trade off, a decision logic process incorporating an up/down counter was used.

The relay performance is investigated using a programmable transmission line (PTL) equipment, from which a series of fault waveforms were applied, corresponding to various line configurations and inception angles for both solid and resistive faults. The relay directional stability was studied for reverse and forward faults.

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LIST OF SYMBOLS

T_w = transformation window width

f_e = extraction frequency

ω_0 = power angular frequency

I = current phasor

V = voltage phasor

a,b,c = phases a, b and c

i(t), v(t) = instantaneous current and voltage

I_p, V_p = current and voltage peak value

$v_1(t)$, $i_1(t)$ = cosine convolution filter transformation components

$v_2(t)$, $i_2(t)$ = sine convolution filter transformation components

$i_{rs}(t)$ = residual current = $i_a(t) + i_b(t) + i_c(t)$

M = residual current compensation factor

i(arc) = arc current

k = discrete variable

$Z_{s\ell}$ = line self impedance

$Z\ell_0$, $Z\ell_1$, $Z\ell_2$ = zero, positive and negative phase sequence impedance

Z_s = source self impedance

Z_{s1}, Z_{s0} = positive and zero source phase sequence impedance

Z_m = mutual impedance

X_m = directional reactance

X_0 = reactance magnitude associated with X_m

Zg = earth return impedance

X_{rs} = scaled reactance at the relay reach

X = line reactance

L = inductance

$h_{1(n)}$, $h_{2(n)}$ = cosine and sine filter impulse responses

$H_1(\omega_0)$, $H_2(\omega_0)$ = cosine and sine convolution filter transfer function

$|H(j\omega)|$ = frequency response magnitude at angular frequency ω

R_f = fault resistance

ϕ_{11}, ϕ_{12} = cosine and sine convolution filter phase shifts at power frequency respectively

z^{-1} = z transform operator

σ = standard deviation

ℓ = line length

α = fault distance p.u.

$K_c K_{ct}$ = primary current scaling factor

$K_v K_{vt}$ = primary voltage scaling factor

T_s = sampling period

* = active low command

$ = hexadecimal format

ϕ_1, ϕ_2 = CCD complementary waveforms

DCL = digital conversion levels

TOP = relay time of operation (ms)

F_{tw} = travelling wave frequency

C_{tw} = travelling wave velocity

CONTENTS

CHAPTER 1

INTRODUCTION

In recent years, there has been a growing trend towards the design and implementation of ultra high speed power system protection, to provide fast fault clearance. The power limits of extra-high-voltage (e.h.v.) transmission lines are governed not only by the operating voltage and maximum current rating but also by system transient stability requirements in abnormal operating conditions such as those resulting from faults on the power system network. Normal maximum load and fault clearing time are related because during a fault, the power flow imbalance within the system causes acceleration and the system becomes unstable if the fault is maintained for too long a period. Reduction in fault clearance time permits more normal power flow and better utilization of transmission networks. The significance of the transmission power gain versus fault clearance speed was revealed by recent studies in North America [1], where a three-phase fault on a 500 kV line near the generator bus with both ends cleared in three-cycles resulted in an 830 MW transfer being stable but an 850 MW transfer being unstable. Similarly 1045 MW was stable for a one-cycle fault clearance but 1100 MW was unstable. The reduction of the fault clearance time from three-cycles to one-cycle allows a gain of 1.26 in power transmission. Alternatively, for a given power flow, faster fault clearance permits a reduction in transmission line interconnections in a system and a subsequent saving in capital investment. A typical single circuit 400 kV overhead line cost approximately £0.4 M/km and considerably more for under-ground cables. In the same study it was revealed that such a gain resulted in estimated typical savings of 29 million dollars

associated with the capital cost of transmitting 1400 MW of power at 500 kV over a distance of 240 km.

At present, the majority of e.h.v. transmission line protection schemes are of the distance protection type, employing conventional phase comparator principles. Such relays have operating times typically of 3/4 a power cycle for faults within the main zone. The slow progress in the field of distance protection is due to the fact that accurate estimation of the fault loop impedance must be achieved entirely in the immediate post fault period, when signal distortion is most severe. Considerable recent research has been conducted into new techniques of directional u.h.s. protection relaying incorporating travelling waves principles [2]. However, directional relaying can only be used in a unit scheme, incorporating communication channels and conventional communication channel delay of typically 15 ms can present limitations to the overall operating time of the scheme. The development of distance protection, with its inherent independence of communication channels, thus continues.

The current objective of the development of power system protection is to produce a fast operating relay, which in conjunction with modern circuit breakers provides one cycle fault clearance. Consideration must be given to the fact that a circuit breaker can interrupt a current only at current zero. For symmetrical 50 Hz systems, the current zeros occur at 10 ms intervals, and for 60 Hz systems, the current zeros occur at 8.3 ms intervals. A modern breaker with 12 ms operating time cannot clear a fault before the second current zero, and relay operating times of less than 4.6 ms and 8.0 ms will produce the same breaker clearing time for 60 Hz and 50 Hz systems respectively. Therefore, for one-cycle

fault clearance, the relay measurement must be completed within less than 4.66 ms and 8 ms for 60 Hz and 50 Hz systems respectively [2, 3 and 4].

For digital protection, the design of filters between the primary transducer and digital processing unit is vital [5]. It is common practice to evaluate algorithms by their frequency response. Much attention has been given to the ability of filters to reject low order harmonics. However, this leads to the choice of slower than necessary algorithms. More attention should be given to the ability to reject travelling wave transients as may be generated by a fault on the protected line. The amplitude and frequency of these disturbances depend mainly on the line length, fault inception angle and source termination [6]. Nevertheless, frequency components above 10 kHz are insignificant and the dominant frequency of travelling waves seldom appear below 600 Hz [7]. Under circumstances where low order harmonics present a problem, a tripping criterion incorporating a successive confirmation of a fault occurrence can be adopted to secure the speed-accuracy trade-off [8].

The continuous development in the field of microcomputers and their support facilities with increasing computational power to price ratio has made the realization of digital distance protection economically viable. The digital realization of power system protection can provide the necessary performance and reliability, since a digital computer is active all the time and self diagnosing can be made to run continuously within the relay. Digital relays are also flexible to use; revision or modification necessitated by changing operating conditions can be easily made.

Distance protection algorithms have evolved over the years. Algorithms based on conventional Fourier Transform techniques [9, 10, 11] are effective in extracting the fundamental components from highly distorted fault waveforms, but their response to a fault is slow. The response of the Fourier Transform method can be improved by using a smaller data window, but small data windows produce problems in current offset conditions and are influenced by high frequency travelling wave components. However, the finite Fourier Transform offers promising performance if used with appropriate filtering. The new technique developed here is a modification of the algorithm which relates the Fourier Transform of a finite window of information, derived from the first order transmission line model measurands of the fault loop impedance. In order to implement the algorithm, a discrete processing technique is used. In this technique samples are fed for individual measurands estimate. A conventional hardware structure has been utilized, which performs the FIR filtering required by the finite Fourier Transform externally to the main digital processor, using analogue CCD tapped delay lines. Each voltage and current relay signal is processed by an individual CCD to extract the Fourier Transform components. In order to reduce the amount of hardware used, the transformed components are multiplexed through a 16-channel analogue multiplexer before conversion to 12-bit digital words (sign + 11 bits). Conventional data transfers using processor interrupts are slow and to meet the 4 kHz sampling rate required for u.h.s. application, a direct memory access (DMA) technique has been used. The evaluation of the discrete process solution requires 16-bit multiplications and since software multiplications are performed in relatively longer times when compared with hardware multipliers, a fast 16-bit multiplier chip has been used. The data transfers to and from the multiplier unit are

performed through a programmable read/write DMA technique. A Z8002 processor manipulates the data and performs the boundary comparison.

The work presented in this thesis concerns the practical implementation of the discrete processing technique, based upon the finite Fourier Transform. A conventional hardware structure is investigated and the new algorithm is tested for single phase to earth faults.

CHAPTER 2

THESIS STRUCTURE

2.1 CHAPTER 3

The most popular distance protection algorithms are described, with their advantages and disadvantages. The distance protection algorithms are categorized into three groups. Firstly, algorithms that determine the phasor voltages and currents at the relaying point, from which the impedance measurements are obtained. Secondly, algorithms which use the Fourier Transform techniques to extract the fundamental components of the relaying voltage and current, from which the impedance can be estimated. Thirdly, algorithms based on the numerical solution of the first order differential equation relating the line parameters R and L to the instantaneous voltage and current.

2.2 CHAPTER 4

The relaying algorithm, which is a modification of the basic algorithm which relates the Fourier Transform of a finite window of information derived from the measurands of the fault loop impedance. The algorithm is implemented using discrete signal processing technique, where samples are fed to the processor for individual impedance estimates.

For the algorithm implementation, a quadrilateral characteristic was used. Following a fault occurrence, the measured impedance converges to the protected zone boundary. The tripping criterion based upon a single impedance estimate can lead to degradation in protection integrity, particularly for a fault near the relay reach. Thus a decision logic process, incorporating an up/down counter was used. The counter is incremented

when the quadrilateral characteristic constraints are satisfied and decremented for out of zone measurements. A trip signal is initiated when the counter reaches a pre set level.

2.3 CHAPTER 5

The process implementation is represented by three distinct operations, the extraction of the Fourier Transform components, the manipulation of the transform components and the decision logic process. Different hardware structures are considered for the process implementation, with respect to speed and accuracy constraints. The process simulation shows that a sampling rate of 4 kHz is required for u.h.s. operation. Consideration is given to the dynamic range of the signal processing scheme.

One possible solution for a full three phase scheme would be to use six parallel microcomputers, to provide three phase-earth and three phase-phase measurements. However, with existing microcomputer technology, such a scheme can only be used with a sampling rate of less than 1 kHz. An alternative hardware structure was chosen, comprising external FIR filters, a microcomputer and a hardware multiplier. Data transfer to and from the microcomputer is performed using direct memory access (DMA) techniques.

2.4 CHAPTER 6

The technical description of the Z8002 microcomputer and the multiplier unit interface are outlined. The 4116 monoboard microcomputer, based on the Z8002 CPU contains the necessary service facilities required by the relay hardware. The functional descriptions of the 4116 microcomputer are outlined briefly.

A software download program was utilised, in order to transfer the Z8002 software code from the host PDP11/23 computer, as necessitated by the relay software development.

The task of generating timing waveforms required to synchronize the relay hardware, is performed using the 4116 board system timer controller (STC). The evaluation of the discrete process solution required the cross-products of the transformed components. As outlined in Chapter 5, the performance of this task requires a hardware multiplier. Data transfer to and from the multiplier is performed using a programmable DMA unit.

The investigation of the discrete process solution requires access to different parts of the algorithm. The development of the relay hardware requires rapid diagnostic tests, using the Z8002 software. These tasks are performed using a 12-bit digital to analogue converter.

2.7 CHAPTER 7

The technical description of the data acquisition unit (DAU) are outlined. The DAU consists of FIR filters, an analogue multiplexer, an analogue to digital converter and a DMA unit.

The FIR filters were realized using charge-coupled-devices (CCD) tapped delay lines. The filter coefficients are adjusted using the taps weighting resistors. The filter impulse responses are governed by the extraction frequency. It was found for a given transformation window width (T_w), an extraction frequency $f_e = 1/2T_w$ is the optimum. The output of the CCD filters are multiplexed using a 16-channel analogue multiplexer. The multiplexed signals are converted to a binary format, using a 12-bit A/D

converter, since it was found that 12-bit resolution satisfies the process accuracy required. The data transfers from the DAU to the microcomputer memory is performed using a DMA unit.

2.6 CHAPTER 8

The relay was tested using a 6 ms transformation window, for 128 km line. The simulated fault waveforms were fed to the relay via a programmable transmission line (PTL) equipment. In order to include the effect of CVT transients, the phase voltages were processed through a CVT simulation program using parameters derived from an actual CVT frequency response.

The relay was tested for solid fault conditions using a single end lumped parameters model, for source termination of 5 GVA or 35 GVA and fault inception angles of 0, 45, 90 and 135 degrees. Primary system waveforms, double end fed, with source terminations of 5 GVA and 35 GVA, in conjunctions with 0, 45, 90 and 135 degree inception angles were also applied to the relay. A series of resistive fault primary system waveforms were applied to the relay using source terminations of 5 GVA and 35 GVA, in conjunction with fault inception angles of 0 and 90 degrees. The fault resistances were 10, 20, 30 and 40 Ω.

The relay directional stability was tested, using the principles of directional reactance, for close-up faults, using 5 and 35 GVA source terminations. The relay forward fault stability was also tested.

For practical purposes, the relaying voltages and currents are set to have equal level for a fault at the reach point. For close-up faults, high source capacity at the relaying point, clipping in the current

signals is inevitable. The relay performance under the current clipping conditions is also studied.

2.7 CHAPTER 9

The relay was tested for a 2 ms transformation window, using the 128 km and 24 km double end fed lines, with fault inception angles of 0 and 90 degrees. With respect to the 24 km line, the relay performance is tested for various SIR, using selected source capacities at the relaying point.

The relay reach accuracy is investigated for both the 128 km and 24 km lines, using the conventional and phase modified Fourier Transform techniques. For a distance protection relay, the overreach increases for high SIR, since the relaying signals can be considerably reduced in magnitude. Thus a level threshold must be applied to restrain the relay operation at low level signals. Two techniques are used to prevent relay operation at low level signal conditions.

A specially developed digital pre-conditioning filter was utilized, the function of which is to eliminate the relaying current exponential offset and to attenuate the travelling wave components subsequent to fault occurrence. The behaviour of the post fault reactance is studied for both 128 km and 24 km lines, using a computer simulation program.

2.8 CHAPTER 10

The work described in this thesis is summarized, with the conclusions obtained from the relay tests. Suggestions for future work are proposed, including optimization of the process implementation.

CHAPTER 3

DISTANCE PROTECTION ALGORITHMS

3.1 REVIEW OF DIGITAL DISTANCE PROTECTION ALGORITHMS

During the past fifteen years, several algorithms for distance protection have been proposed, based on real time impedance measurement. Nevertheless these algorithms can be categorized into three groups.

The first group is comprised of algorithms to determine the phasor voltage V and current I at the relaying point, so that the impedance seen by the relay is given by:

$$|Z| = \frac{V_p}{I_p} = R + jX \qquad \text{--- 3.1}$$

where R and X are the resistance and reactance of the line respectively.

The second group consists of algorithms which use the Fourier Transform techniques to extract the fundamental components of the relaying voltages and currents.

The last group consists of algorithms based on a numerical solution of the first order differential equation relating the line parameters R and L to the instantaneous voltage v(t), and current i(t), i.e.:

$$v(t) = R\, i(t) + L \frac{di(t)}{dt} \qquad \text{--- 3.2}$$

where R and L are the resistance and inductance respectively of the line between the relaying end and the fault.

3.1.1 Relaying signal peak measurements

In this method, the impedance estimation involves the predictive measured value of the peak voltage and current. Consider a pure sinusoidal current signal of frequency ω_0 then:

$$i(t) = I_p \, SIN(\omega_0 t) \qquad \text{--- } 3.3$$

where $i(t)$ is the instantaneous current value at time t and I_p is the peak current value. The rate of change of the current at any instant is given by:

$$i'(t) = I_p \, \omega_0 \, COS(\omega_0 t) \qquad \text{--- } 3.4$$

One can see that when $i(t) = 0$, $i'(t)$ assumes its maximum value; thus the rate-of-change at the zero crossing is a good indication of the peak value. The impedance measurements made by predicting the peak value of signals from the rate of change is acceptable for pure sinusoidal signals. However, the measured impedance using this technique is often subject to considerable error, since following a fault, the signal distortion is most severe.

Mann *et al* [12] utilized the fact that the peak value can be measured by using the instantaneous sample value and its derivative. Squaring and adding Eqns. 3.3 and 3.4 thus gives:

$$I_p^2 = i^2(t) + \left[\frac{i'(t)}{\omega_0}\right]^2 \qquad \text{--- } 3.5$$

and the phase difference between the current and the voltage is given by Eqn. 3.6:

$$\phi = \text{ARCTAN} \frac{i(t)\,\omega_0}{i'(t)} - \text{ARCTAN} \frac{v(t)\,\omega_0}{v'(t)} \qquad \text{--- } 3.6$$

Eqns. 3.5 and 3.6 enable the complete impedance measurements in phase and magnitude to be accomplished. In order to avoid excessive differentiation error due to noise, a digital smoothing has been used. Indeed digital filtering improves the impedance measurement accuracy, but the exponential offset causes ill-behaviour of the algorithm.

Gilcrest *et al* [13] modified the Mann and Morrison algorithm by using the first and second differences of v(t) and i(t) rather than the raw sample value and its first differences. The impedance seen at the relaying point is then given by:

$$|Z|^2 = \frac{(\acute{v}(t))^2 + (\tilde{v}(t)/\omega_0)^2}{(\acute{i}(t))^2 + (\tilde{i}(t)/\omega_0)^2} \qquad \text{--- 3.7}$$

and the impedance angle is given by Eqn. 3.8.

$$\phi = \text{ARCTAN}\frac{i(t)\,\omega_0}{\tilde{i}(t)} - \text{ARCTAN}\frac{v(t)\,\omega_0}{\tilde{v}(t)} \qquad \text{--- 3.8}$$

The differences of the voltage and current are found from the sampled data:

$$\acute{i}(t) = \frac{1}{2T_s}\left(i(k+1) - i(k-1)\right) \qquad \text{--- 3.9}$$

and

$$\tilde{i}(t) = \frac{1}{2T_s}\left(i(k-1) - 2i(k) + i(k-1)\right) \qquad \text{--- 3.10}$$

where i(k-1), i(k), i(k+1) are the magnitude of successive samples and T_s is the sampling interval. The main benefit of this algorithm is that a constant d.c. offset has no effect, since it is removed by the difference expressions. Thus an exponential offset has minimal effect on the algorithm. The disadvantage of the algorithm is that the high frequency components of the first and second differencing produces more error when

compared with the Mann and Morrison algorithm [14].

The peak measurement schemes have been largely abandoned due to the algorithm deficiency, which assumes that the waveforms presented to the relay are pure sinusoids.

3.1.2 Fourier methods

These methods depend on extracting the fundamental components of the current and voltage from the fault transients. This can be achieved by correlating the voltage and current samples with stored samples of reference fundamental sine and cosine waveforms.

The process of extracting the fundamental components, using the Fourier Transform technique can be represented in the form of Eqns. 3.11 and 3.12:

$$A = \frac{2}{N} \sum_{k=0}^{N} f(t-kT_s)\ \mathrm{COS}(\omega_0 kT_s) \qquad \text{--- } 3.11$$

$$B = \frac{2}{N} \sum_{k=0}^{N} f(t-kT_s)\ \mathrm{SIN}(\omega_0 kT_2) \qquad \text{--- } 3.12$$

where T_s is the sample interval and N is the number of samples in the correlation window. The magnitude C and the phase of the fundamental components are given by:

$$C = [A^2 + B^2]^{1/2} \qquad \text{--- } 3.13$$

and

$$\phi = \mathrm{ARCTAN}\ \frac{B}{A} \qquad \text{--- } 3.14$$

The modulus and argument of the system impedance can be estimated from

the sample voltage and current waveform using:

$$|Z| = \frac{C_v}{C_i} \qquad \text{--- 3.15}$$

$$\text{Arg}(Z) = \phi_v - \phi_i \qquad \text{--- 3.16}$$

Fig.3.1 shows the process block diagram.

Ramamoory [9] suggested that the desired fundamental voltage and current can be extracted by correlating a full-cycle of data sample window with sinusoidal and cosinusoidal reference waveforms, i.e. $NT_s = 1/f_0$. The general expression for the cosine $v_1(k)$ and sine $v_2(k)$ components of the voltage at a sample k is given by Eqns. 3.17 and 3.18.

$$v_1(k) = \frac{1}{N}\left[v(k-N) + v(k) + 2\sum_{\ell=1}^{N-1} v(k+N+\ell)\ \text{COS}\left(\frac{2\pi}{N}\ell\right)\right] \qquad \text{--- 3.17}$$

$$v_2(k) = \frac{1}{N}\left[2\sum_{\ell-1}^{N-1} v(k+N+\ell)\ \text{SIN}\left(\frac{2\pi}{N}\ell\right)\right] \qquad \text{--- 3.18}$$

Fig.3.2 shows the frequency response of full-cycle data window [14]. It should be noted that, theoretically, the full-cycle Fourier Transform promises the best accuracy because it utilizes the fundamental components only and all other components in the fault frequency spectrum are rejected. However, this technique provides a drastic filtering and the filter output is damped, consequently leading to a slow convergence toward the post fault impedance measurement.

In order to improve the time response of the algorithm, Phadke *et al* [10] suggested the reduction of the data window to one-half a fundamental cycle. The shortened data window technique improves the filter response,

hence a faster convergence toward the post fault impedance estimate, but additional error due to exponential offset has been encountered. Fig.3.3 shows the process frequency response [14]. In order to remedy the algorithm performance Phadke suggested that the magnitude of the exponential offset is determined by the line X/R ratio, and implied that the magnitude of the exponential offset subtracted from the fault waveform prior to the Fourier Transform.

3.1.3 Algorithms based on system parameters differential equation

As mentioned previously, these algorithms assume a transmission line model consists of series inductance and resistance elements:

$$v(t) = R\, i(t) + L \frac{di(t)}{dt} \qquad \text{--- } 3.19$$

Since the form of the differential equation for this model is known, the incoming voltage and current samples can be regarded as a series, the solution of which can be used to find the line parameters. This model has the advantage of recognising the exponential offset as a valid component.

McInnes *et al* [15] proposed a solution to estimate the line parameters by integrating over two successive time periods and solving the resulting simultaneous linear equations. The sampled data expressions are:

$$L(k) = \frac{T_s}{2} \frac{[v(k-1)+v(k-2)][i(k-1)+i(k)] - [v(k-1)+v(k)][i(k-1)+i(k-2)]}{[i(k-1)+i(k)][i(k-1)-i(k-2)] - [i(k-1)+i(k-2)][i(k)-i(k-1)]} \qquad \text{--- } 3.20$$

$$R(k) = \frac{[v(k-1)+v(k)][i(k-1)+i(k-2)] - [v(k-1)+v(k-2)][i(k)+i(k-1)]}{[i(k-1)+i(k)][i(k-1)-i(k-2)] - [i(k-1)+i(k-2)][i(k)-i(k-1)]} \qquad \text{--- } 3.21$$

The above algorithm has been modified since originally proposed by McInnes and Morrison and different solutions have been suggested.

Sanderson *et al* [7] proposed a solution of Eqn. 3.2 in the form:

$$v(t) = R\, i(t) + L\, i'(t) \qquad \text{--- } 3.22$$

$$v'(t) = R\, i'(t) + L\, i''(t) \qquad \text{--- } 3.23$$

The use of the first and second differentiation accentuates noise in the measured parameters. In order to improve the system noise immunity, a digital smoothing process has been suggested by fitting a second order polynomial to a data window of seven samples as proposed by Savitzky *et al* [16]. The estimates of v(k+3) and i(k+3) (denoted by y) is given by:

$$y0 = \frac{1}{21}[-2[y(k+3)+y(k-3)]+3[y(k+2)+y(k-2)]+6[y(k+])+y(k-1)]+7y(k)]$$

$$= A0\ \ Y0 \qquad \text{--- } 3.24$$

$$y'0 = \frac{1}{28T_s}[3[y(k+3)+y(k-3)]+2[y(k+2)+y(k-2)+[y(k+])+y(k-1)]$$

$$= A1\ \ Y1 \qquad \text{--- } 3.25$$

$$y''0 = \frac{1}{24T_s^2}[5[y(k+3)+y(k-3)]-3[y(k+2)+y(k-2)-4y(k)]$$

$$= A2\ \ Y2 \qquad \text{--- } 3.26$$

And the line parameter formulations are then:

$$L(k+3) = k1\ \frac{V0\ I1 - V1\ I0}{I1^2 - (k2\ I2)\ I0} \qquad \text{--- } 3.27$$

$$R(k+3) = \frac{V1\ I1 - (k2\ I2)\ V0}{I1^2 - (k2\ I2)\ I0} \qquad \text{--- } 3.28$$

where k1 and k2 are the first and second differentiation error compensation factors. The disadvantage of the curve fitting technique is that it requires at least seven samples of data window, which inevitably slows the process response and it also restricts the sampling rate to a certain value (833 Hz).

Varga *et al* [17] proposed a solution of Eqn. 3.19 by integrating over two consecutive time intervals t0-t1 and t1-t2 in the form:

$$\int_{t0}^{t1} v\,dt = L\,[i(t1) - i(t0)] + R \int_{t0}^{t1} i\,dt \qquad \text{--- } 3.29$$

$$\int_{t1}^{t2} v\,dt = L\,[i(t2) - i(t1)] + R \int_{t1}^{t2} i\,dt \qquad \text{--- } 3.30$$

The integration in Varga's approach is simply a moving average process over two rectangular windows, the second window h2 is shifted in time relative to the first window h1 as shown in Fig.3.4. Each window h1 and h2 has six samples and the middle sample is common for both windows and the current differentials $i'1(t)$ and $i'2(t)$ become simply the difference between the first and the last samples in the moving average windows h1 and h2. The advantage of using a rectangular window is that all the samples in the algorithm window are supplied to the algorithm without modification, while in all other filters the window samples have to be scaled individually by the filter coefficients. However, the frequency response peaks in between the filter zeros are of greater magnitude compared with the sine or cosine window [14] as shown in Fig.3.5. The disadvantage of using time shifted rectangular windows is that the second window h2 has a delayed response to the post fault data which causes a

slow relay operation.

Wiszniewski [11] shows that the window length affects the frequency spectra of the Fourier Transform process. With the decrease of the window length T_w, the frequency components spectra increase. The Fourier Transform convolution integral can be written in the form:

$$I(\omega_0) = \int_0^{T_w} i(\tau)\ \exp(-j\omega\tau)\ d\tau = I(\omega_0) + Ia(\omega) + Ip(\omega) \qquad \text{--- 3.31}$$

where $I(\omega_0)$ is the Fourier Transform fundamental component, $Ia(\omega)$ is the Fourier Transform of the exponential component and $Ip(\omega)$ is the frequency component induced by travelling waves. As long as the data window T_w is greater or equal to one cycle of the fundamental component of period T_0, the error introduced by the data window, $Ia(\omega)$ and $Ip(\omega)$ is very small. However, if the data window is smaller than one fundamental period, the transient error is increased and Wiszniewski advocates the correlation of the data window with reference sine and cosine of frequency f_e that is related to the data window:

$$f_e = \frac{1}{T_w} \qquad \text{--- 3.32}$$

and the line parameters formulation is given by:

$$R^2(t) = \frac{k^2 i_1(t)\ v_1(t) + p^2 i_2(t)\ v_2(t)}{k^2 i_1(t) + p^2 i_2(t)} \qquad \text{--- 3.33}$$

$$X^2(t) = \frac{k\ p\ i_2(t)\ v_1(t) + k\ p\ i_1(t)\ v_2(t)}{k^2 i_1(t) + p^2 i_2(t)} \qquad \text{--- 3.34}$$

where subscripts 1 and 2 refer to the cosine and sine components extracted from correlating with reference cosine and sine of frequency $1/T_w$. The terms k and p are the error coefficients for the cosine and

sine components of the Fourier Transform respectively. The terms k and p are determined from the data window length as given by Eqns. 3.35 and 3.36.

$$k = \frac{\pi(1 - r^2)}{r \, SIN(\pi r)} \qquad \text{--- } 3.35$$

$$p = - \frac{(1 - r^2)}{SIN(\pi r)} \qquad \text{--- } 3.36$$

where

$$r = \frac{f_0}{f_e} \qquad \text{--- } 3.37$$

Wiszniewski acknowledges that this method is effective in minimizing the error due to the exponential offset, but the error due to the travelling waves is accentuated. In this respect it must be noted that the first order differential equation utilizing 50 Hz parameters is not acceptable over the whole range of frequencies, and therefore the algorithm accuracy is affected.

3.2 SUMMARY

The most popular distance protection algorithms with their advantages and disadvantages are presented in this Chapter.

Algorithms based on the peak voltage and current determination, assume that the waveforms presented to the relay are pure sinusoids. The resulting measured impedance are severely distorted by harmonics.

Algorithms based on Fourier Transform analysis are effective in extracting the fundamental components from a highly distorted fault waveforms. However, their response to a fault is slow and is somewhat affected by

the presence of exponential offset components.

The line parameters differential equation, provides a faster response to a fault, if an appropriate filtering of the relaying signals is used. It also recognizes the exponential offset as a valid component.

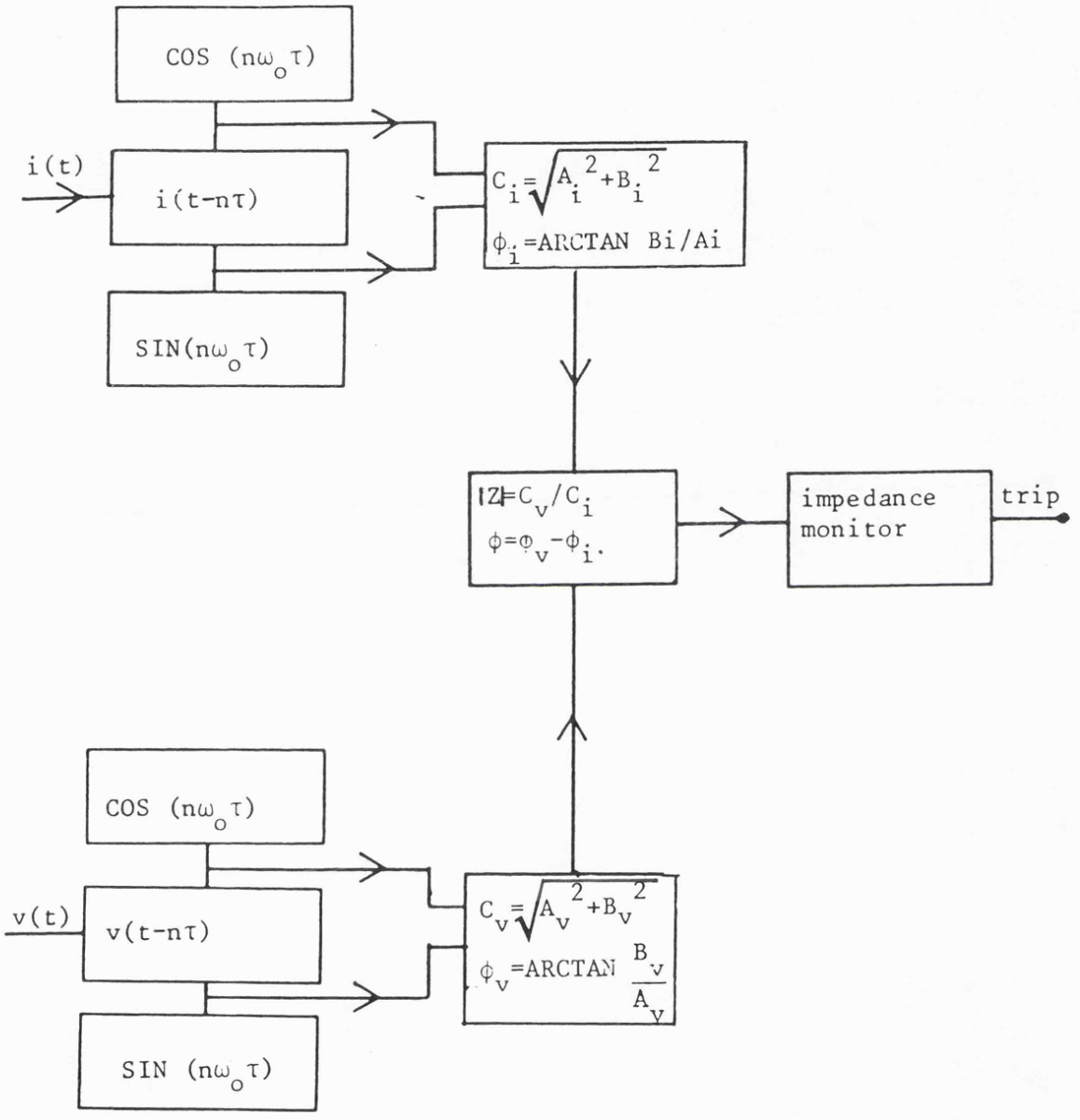


Fig. 3.1 : Fourier transform process

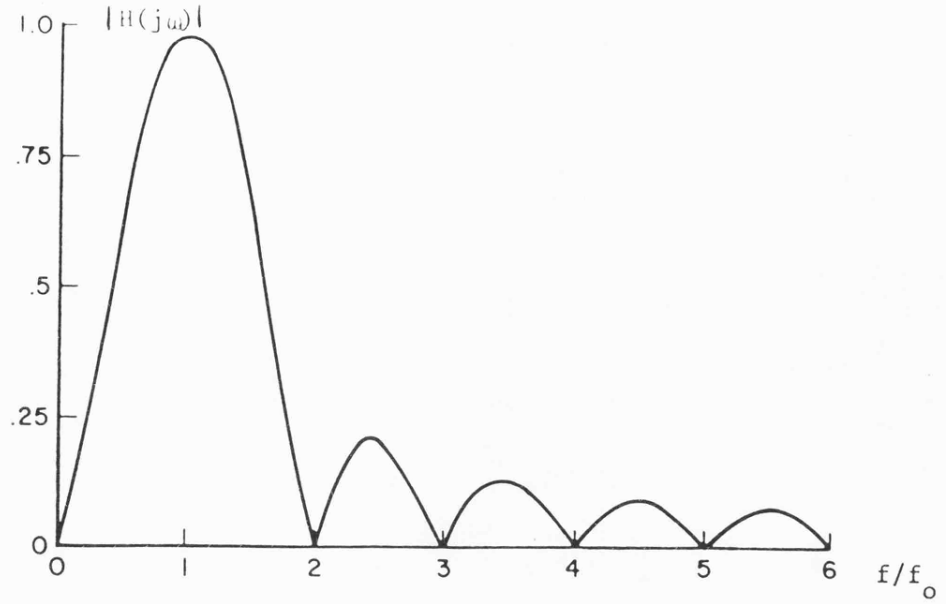


Fig. 3.2 : Frequency response of the full-cycle Fourier Transform algorithm (12 samples per cycle)

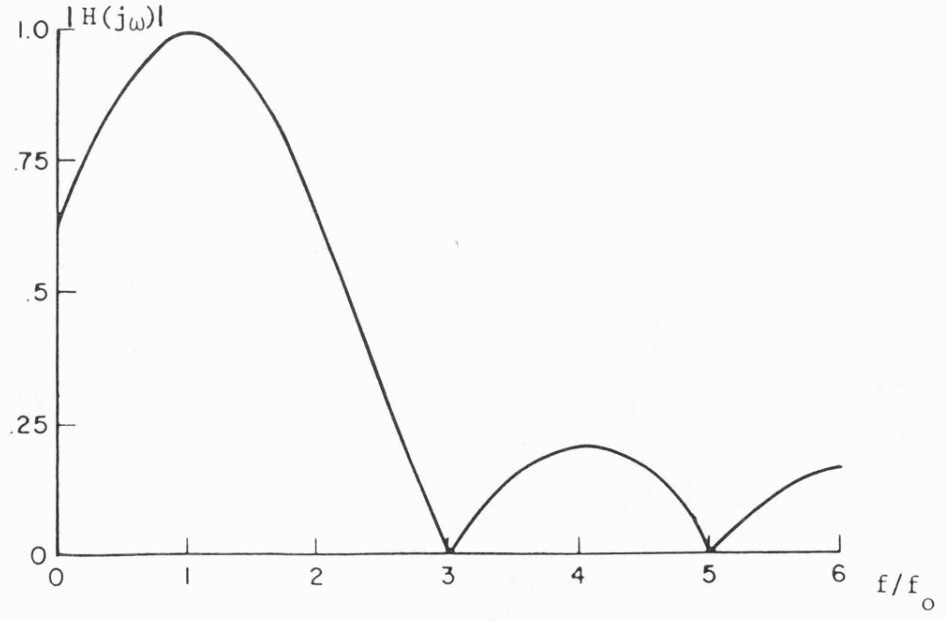


Fig. 3.3 : Frequency response of Fourier Transform algorithm with half a power cycle data window (12 samples per cycle)

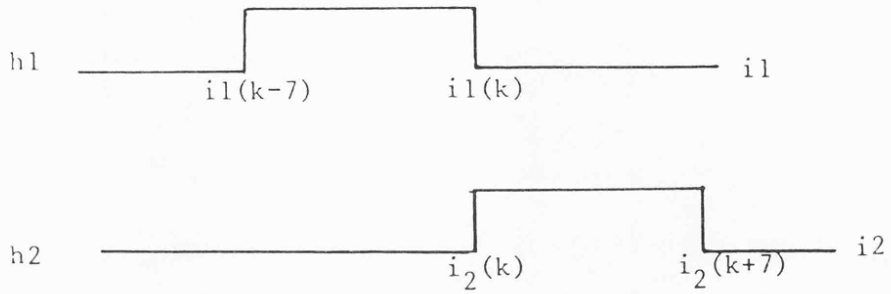


Fig. 3.4 : Two time shifted rectangular windows

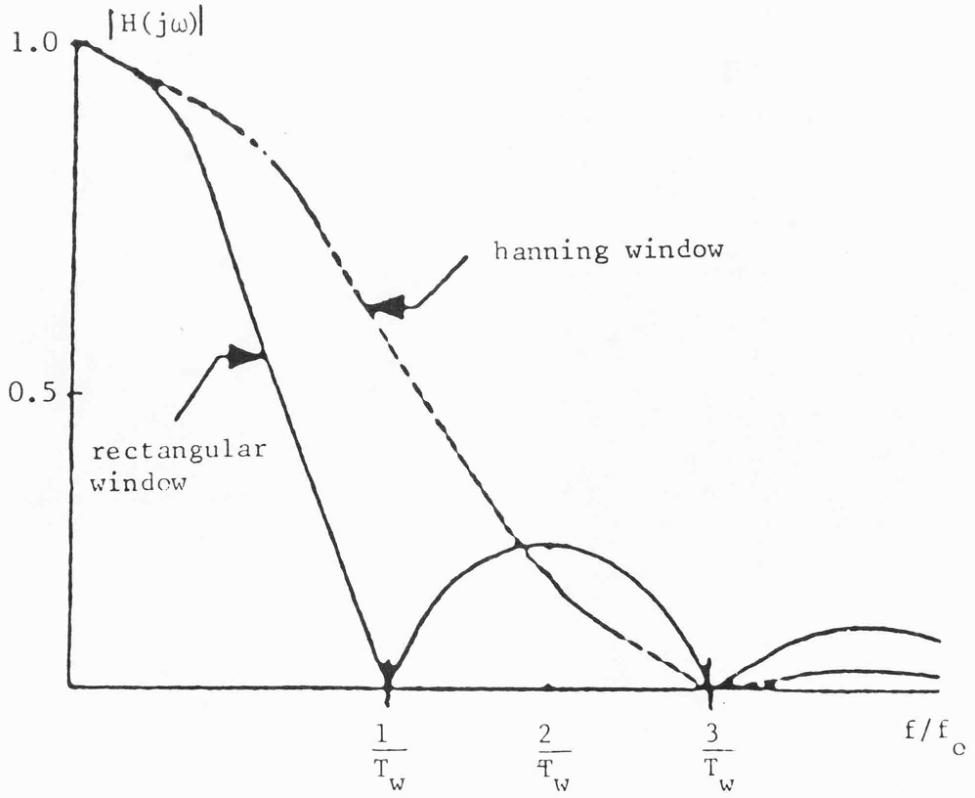


Fig. 3.5 : Leakage peak comparison for rectangular and hanning window (half a sine wave impulse response)

CHAPTER 4

FINITE TRANSFORM DISTANCE PROTECTION ALGORITHM

4.1 THE DISTANCE PROTECTION SCHEME ALGORITHM

The current distance protection scheme is a modification of the basic algorithm which relates the Fourier Transform of a finite window of information derived from the measurands to the fault loop impedance [4, 18 and 19].

Consider the first order transmission line model as shown in Fig. 4.1, where the relation between the instantaneous relaying voltage v(t) and current i(t) is given by the expression,

$$v(t) = R\, i(t) + L \left(di(t)/d(t)\right) \qquad \text{--- 4.1}$$

Application of the finite Fourier Transform filtering defined by the convolution integral gives:

$$\overline{v(t)} = \int_0^{T_w} v(t-\tau)\, h(\tau)\, d(\tau) \qquad \text{--- 4.2}$$

where $h(\tau)$ is the filter impulse response. Applying the convolution of Eqn. 4.2, Eqn. 4.1 transforms to Eqn. 4.3:

$$\overline{v(t)} = R\, \overline{i(t)} + L\, \overline{\left(di(t)/d(t)\right)} \qquad \text{--- 4.3}$$

In Eqn. 4.3, the term $\overline{i(t)}$ is the filtered version of the current signal and $\overline{(di/dt)}$ is the filtered version of the differentiated current signal i(t). Using the linear system differentiability principle, i.e. $\overline{\left(i'(t)\right)} = \overline{\left(i(t)\right)}'$, Eqn. 4.3 can be written in the form of Eqn. 4.4:

$$\overline{v(t)} = R\ \overline{i(t)} + L\ (d/dt)\ \overline{i} \qquad \text{--- 4.4}$$

Consider two filters having impulse responses $h_1(\tau)$ and $h_2(\tau)$, defined over the same window width T_w. Eqn. 4.2 gives the following forms:

$$\overline{v_1(t)} = \int_0^{T_w} v(t-\tau)\ h_1(\tau)\ d(\tau) \qquad \text{--- 4.5}$$

$$\overline{v_2(t)} = \int_0^{T_w} v(t-\tau)\ h_2(\tau)\ d(\tau) \qquad \text{--- 4.6}$$

Defining the filter impulse responses $h_1(\tau)$ and $h_2(\tau)$ as $COS(\omega\tau)$ and $SIN(\omega\tau)$ respectively, Eqns. 4.5 and 4.6 expand to the form of Eqns. 4.7 and 4.8.

$$\overline{v_1(t)} = \int_0^{T_w} v(t-\tau)\ COS(\omega\tau)\ d(\tau) \qquad \text{--- 4.7}$$

$$\overline{v_2(t)} = \int_0^{T_w} v(t-\tau)\ SIN(\omega\tau)\ d(\tau) \qquad \text{--- 4.8}$$

Alternatively Eqns. 4.7 and 4.8 can be written in the following way.

$$\overline{v(t)} = \overline{v_1(t)} + j\overline{v_2(t)} \qquad \text{--- 4.9}$$

and

$$\overline{v(t)} = \int_0^{T_w} v(t-\tau)\ EXP\ (-j\omega\tau)d(\tau) \qquad \text{--- 4.10}$$

For simplicity, the filtering symbol (———) will be omitted.

Application of Eqns. 4.7 and 4.8 to Eqn. 4.4 gives:

$$v_1(t) = R\, i_1(t) + L\, i_1'(t) \qquad \text{--- 4.11}$$

$$v_2(t) = R\, i_2(t) + L\, i_2'(t) \qquad \text{--- 4.12}$$

which may be written in the matrix form of Eqn. 4.13.

$$\begin{bmatrix} v_1(t) \\ \\ v_2(t) \end{bmatrix} = \begin{bmatrix} i_1(t) & i_1'(t) \\ \\ i_2(t) & i_2'(t) \end{bmatrix} \begin{bmatrix} R \\ \\ L \end{bmatrix} \qquad \text{--- 4.13}$$

Inverting the matrix 4.13 to solve for R and L gives:

$$\begin{bmatrix} R \\ \\ L \end{bmatrix} = \frac{1}{D(t)} \begin{bmatrix} i_2'(t) & -i_1'(t) \\ \\ -i_2(t) & i_1(t) \end{bmatrix} \begin{bmatrix} v_1(t) \\ \\ v_2(t) \end{bmatrix} \qquad \text{--- 4.14}$$

where the determinant term is given by Eqn. 4.15.

$$D(t) = i_1(t)\, i_2'(t) - i_1'(t)\, i_2(t) \qquad \text{--- 4.15}$$

The block diagram of the time domain matrix solution is shown in Fig. 4.2. R and L are given by Eqns. 4.16 and 4.17.

$$R = \frac{v_1(t)\, i_2'(t) - v_2(t)\, i_1'(t)}{D(t)} \qquad \text{--- 4.16}$$

$$L = \frac{v_2(t)\, i_1(t) - v_1(t)\, i_2(t)}{D(t)} \qquad \text{--- 4.17}$$

4.1.1 Discrete processing solution

The need for faster and consistent tripping times prompted an interest in discrete processing techniques. In this technique, samples are fed to the process for individual impedance estimates. The filtered current

and voltage in Eqns. 4.11 and 4.12 can be made available as samples (using the discrete variable k), at intervals T_s in time. Since a given sample value contains no information about the derivative at the sampling instant, the derivative can be approximated by computing the difference between the current and previous samples. The differentiated current is then expressed [20]:-

$$i_1'(k) = (1/T_s)\,[i_1(k) - i_1(k-1)] \qquad \text{--- } 4.18$$

$$i_2'(k) = (1/T_s)\,[i_2(k) - i_2(k-1)] \qquad \text{--- } 4.19$$

where i(k-1) and i(k) represent the previous and current samples respectively. Eqns. 4.11 and 4.12 can thus be written in the discrete form of Eqns. 4.20 and 4.21.

$$v_1(k) = R\,i_1(k) + (L/T_s)\,\left(i_1(k) - i_1(k-1)\right) \qquad \text{--- } 4.20$$

$$v_2(k) = R\,i_2(k) + (L/T_s)\,\left(i_2(k) - i_2(k-1)\right) \qquad \text{--- } 4.21$$

Eqns. 4.20 and 4.21 arrange in the matrix form as:

$$\begin{bmatrix} v_1(k) \\ v_2(k) \end{bmatrix} = \begin{bmatrix} i_1(k) & -i_1(k-1) \\ i_2(k) & -i_2(k-1) \end{bmatrix} \begin{bmatrix} R+L/T_s \\ L/T_s \end{bmatrix} \qquad \text{--- } 4.22$$

Inversion of the matrix leads to Eqns. 4.23 and 4.24.

$$\begin{bmatrix} R+L/T_s \\ L/T_s \end{bmatrix} = \frac{1}{D(k)} \begin{bmatrix} -i_2(k-1) & i_1(k-1) \\ -i_2(k) & i_1(k) \end{bmatrix} \begin{bmatrix} v_1(k) \\ v_2(k) \end{bmatrix} \qquad \text{--- } 4.23$$

$$D(k) = i_1(k-1)\,i_2(k) - i_1(k)\,i_2(k-1) \qquad \text{--- } 4.24$$

The block diagram to implement the discrete process is shown in Fig. 4.3. Figs. 4.4a, 4.4b and 4.4c show the overall discrete processing technique schematic diagrams. Fig. 4.4a shows the relaying current signal formation including the residual current compensation required for phase-earth faults (see Appendix 1). Fig. 4.4b shows the relaying voltage signal formation. Fig. 4.4c shows the manipulation of the relaying signals for the six types of fault required by conventional distance relays phase-earth faults a-e, b-e, c-e and phase-phase faults a-b, b-c and c-a.

4.2 PRODUCTION OF QUADRILATERAL CHARACTERISTIC

A conventional distance relay characteristic defines the region where the fault loop impedance converges after fault inception on a transmission line. It is usually plotted on an impedance diagram with R and jX axes. A typical distance characteristic has two selective functions such as [21]:

a-Direction, which means that tripping is confined to the first quadrant of the impedance plane, although some incursions into other quadrants are permissible.

b-Selectivity, which means that the relay is not prone to maloperations during a power swing condition, since the measured impedance is reduced to a level comparable with that of a high resistance fault. Although the current distance protection scheme is not based on conventional impedance measurement, a similar characteristic can be adopted as shown in Fig. 4.5. For the quadrilateral characteristic shown, a trip signal is initiated if:

$$-X_0 < \omega_0 L < X_r \qquad \text{--- 4.25}$$

$$R_0 < R < R_r + K_1 \omega_0 L \qquad \text{--- 4.26}$$

where $K_1 = \text{COT}\underline{|Z\ell_1}$. The term X_0 in Fig. 4.5 is associated with the directional reactance (X_m), which is described in detail in Chapter 8. Multiplying Eqn. 4.25 by D(k) and dividing by ($\omega_0 T_s$) gives Eqn. 4.27.

$$(-X_0/\omega_0 T_s)\ [D(k)] < [LD(k)/T_s] < (X_r/\omega_0 T_s)\ [D(k)] \qquad \text{--- 4.27}$$

Multiplying Eqn. 4.26 by D(k) gives Eqn. 4.28.

$$(R_0)\ [D(k)] < [RD(k)] < R_r\ [D(k)] + (K_1 \omega_0 T_s)\ [LD(k)/T_s] \qquad \text{--- 4.28}$$

To solve Eqns. 4.27 and 4.28, the terms D(k), $LD(k)/T_s$ and $(R+L/T_s)D(k)$ are obtained directly from expression 4.23 as follows:

$$D(k) = i_2(k)\ i_1(k-1) - i_1(k)\ i_2(k-1) \qquad \text{--- 4.29}$$

$$(R+L/T_s)\ D(k) = v_2(k)\ i_1(k-1) - v_1(k)\ i_2(k-1) \qquad \text{--- 4.30}$$

$$LD(k)/T_s = v_2(k)\ i_1(k) - v_1(k)\ i_2(k) \qquad \text{--- 4.31}$$

The term RD(k) in Eqn. 4.28 is formulated from Eqns. 4.30 and 4.31. Eqn. 4.30 can be written in the following form:

$$RD(k) = \{v_2(k)\ i_1(k-1) - v_1(k)\ i_2(k-1)\} - LD(k)/T_s \qquad \text{--- 4.32}$$

$$RD(k) = (R+L/T_s)D(k) - LD(k)/T_s \qquad \text{--- 4.33}$$

Eqns. 4.27 and 4.28 can be simplified in the form of Eqns. 4.34 and 4.35.

$$K_3\ [D(k)] < [LD(k)/T_s] < K_4\ [D(k)] \qquad \text{--- 4.34}$$

$$R_0\ [D(k)] < [RD(k)] < R_r\ [D(k)] + K_5\ [LD(k)/T_s] \qquad \text{--- 4.35}$$

where the constants K_3, K_4 and K_5 and their corresponding numerical values (see Appendix 2) are given as follows:

$$K_3 = -X_0/(\omega_0 T_s) = -0.429 \quad \text{---} \quad 4.36$$

$$K_4 = X_r/(\omega_0 T_s) = 8.43 \quad \text{---} \quad 4.37$$

$$K_5 = K_1(\omega_0 T_s) = 0.008 \quad \text{---} \quad 4.38$$

4.3 DECISION LOGIC

The measured impedance is compared with the pre-determined characteristic of impedance which specifies a zone in the impedance plane. The tripping criterion, which is based on single impedance estimate can lead to the degradation in protection integrity because, in practice, significant fluctuation in impedance estimates occur after fault inception. Algorithm simulation shows that a fault just beyond the relay reach can cause impedance estimates falling within the relay characteristic boundary [8]. The impedance transients can be illustrated for voltage maximum faults, where the relaying voltage signals are severely contaminated by travelling wave harmonics, and voltage minimum faults where the impedance estimates show a downward transient droop.

In order to maintain relay stability, a decision process criterion incorporating an up/down counter is used. The counter is incremented when an impedance estimate lies inside the protection zone characteristic boundary, and decremented for impedance estimates outside the protected zone. A trip signal is initiated when the counter reaches a pre-determined level of 5 counts. This technique reduces the relay operating times for faults near the zone boundary. However, the trip times can be

improved for faults well inside the protected zone boundary by utilizing a second region in the impedance plane (the inner region) which is set to 75% of the reactance reach as shown in Fig. 4.5. The inner region controls the magnitude of the counter increments. Impedance estimates inside the inner region cause the counter to increment by 2. It is important to note that the inner region can be allowed to overreach, but this must not extend beyond the main zone boundary. Fig. 4.6 shows the decision logic process flow chart.

4.4 EVALUATION OF THE DISCRETE MATRIX SOLUTION

The solution of expression 4.23, which gives R and L estimates, involves products of the transformed relaying signals. The filters $h_1(\tau)$ and $h_2(\tau)$ must be designed so that both R and L estimates are well behaved and stabilize quickly after a fault inception. The matrix can be evaluated by studying the behaviour of the term D(t), since it affects the estimation of both R and L. It is desired that this term is unipolar, since if it approaches zero, the solution of the matrix will be ill behaved, and if it becomes negative, the relay quadrilateral boundary comparison, Eqns. 4.34 and 4.35, will be in error. It will be shown that this is of concern in the event of the relaying currents exponential offsets.

4.4.1 D(t) behaviour

As shown in Appendix 3, for pure sinusoidal current signals, D(t) can be expressed in the form:

$$D(t) = |H_1(\omega_0)|\ |H_2(\omega_0)|\ I_p^2\ \mathrm{SIN}(\phi_{11}-\phi_{12})\ \mathrm{SIN}(\omega_0 T_s) \qquad \text{--- } 4.39$$

where ϕ_{11} and ϕ_{12} are the phase shift of the filters $H_1(\omega_0)$ and $H_2(\omega_0)$ respectively at a frequency ω_0. Eqn. 4.39 clearly shows that D(t) is

a d.c. term for pure sinusoidal current signals, and its magnitude is a function of the filter phase shift $\underline{|(\phi_{11}-\phi_{12})}$ which is a maximum for $\underline{|(\phi_{11}-\phi_{12})} = \pi/2$. Its magnitude is also a function of the current signal magnitude I_p. In the event of an exponential current offset, D(t) can be expressed in the form of Eqn. 4.40 (see Appeneix 3).

$$D(t) = D_{ss} + D_{off} \qquad \text{--- } 4.40$$

where the term D_{ss} is the auto-product for a pure sinusoidal input as given by Eqn. 4.39, and D_{off} is the sinusoidal component derived from the exponential offset.

In order to investigate the behaviour of D(k) in practice, the circuit shown in Fig. 4.7 was utilized. A variable cut off frequency low-pass filter introduces a 90 degree phase shift, i.e. $\underline{|(\phi_{11}-\phi_{12})}$. The two operational amplifiers are used to analyse the behaviour of D(k) under d.c. offset conditions. The phase shifted signal components are converted to 12-bit digits and fed to a microcomputer, which manipulate the signal samples to establish D(k). The established D(k) term is converted to an analogue signal using 12-bit digital-to-analogue conversion. With respect to the above described test it must be noted that the signal components I_{p1} and I_{p2} are of equal magnitude. In practice, the magnitude of the current signal components I_{p1} and I_{p2} are dictated by the gain of the two filters, $H_1(\omega_0)$ and $H_2(\omega_0)$. However, this technique gives a D(k) magnitude different from that of actual D(k) estimate. Fig. 4.8 shows a practical observation of D(k), with the filter phase shift fixed at 90 degree, i.e. $\underline{|(\phi_{11}-\phi_{12})} = \pi/2$ and an a.c. input signal of a 10 V p.p. For a pure sinusoidal input, D(k) maintains a d.c. level. When a d.c. offset of 1 V is added, using the operational amplifiers in Fig. 4.7,

D(k) develops a sinusoidal component of one power frequency, imposed on the D(k) d.c. level. As the added d.c. offset is increased, the D(k) sinusoidal component magnitude increased and when the d.c. offset is 3.0 V the D(k) sinusoidal component achieves a negative value. At this stage it is essential to reduce the d.c. offset to ensure that D(k) remains unipolar, since the constraints involving D(k) in Eqns. 4.34 and 4.35 are not satisfied if D(k) goes negative. This has been achieved by using a high-pass filter of cut-off frequency chosen to be 4 Hz.

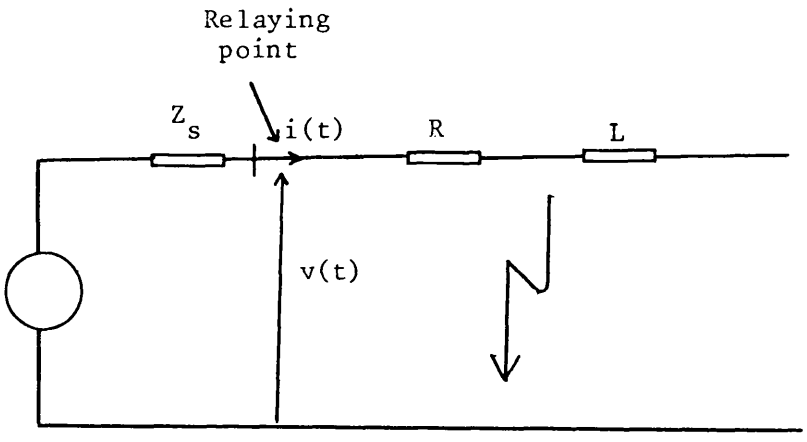


Fig. 4.1 : Transmission line model

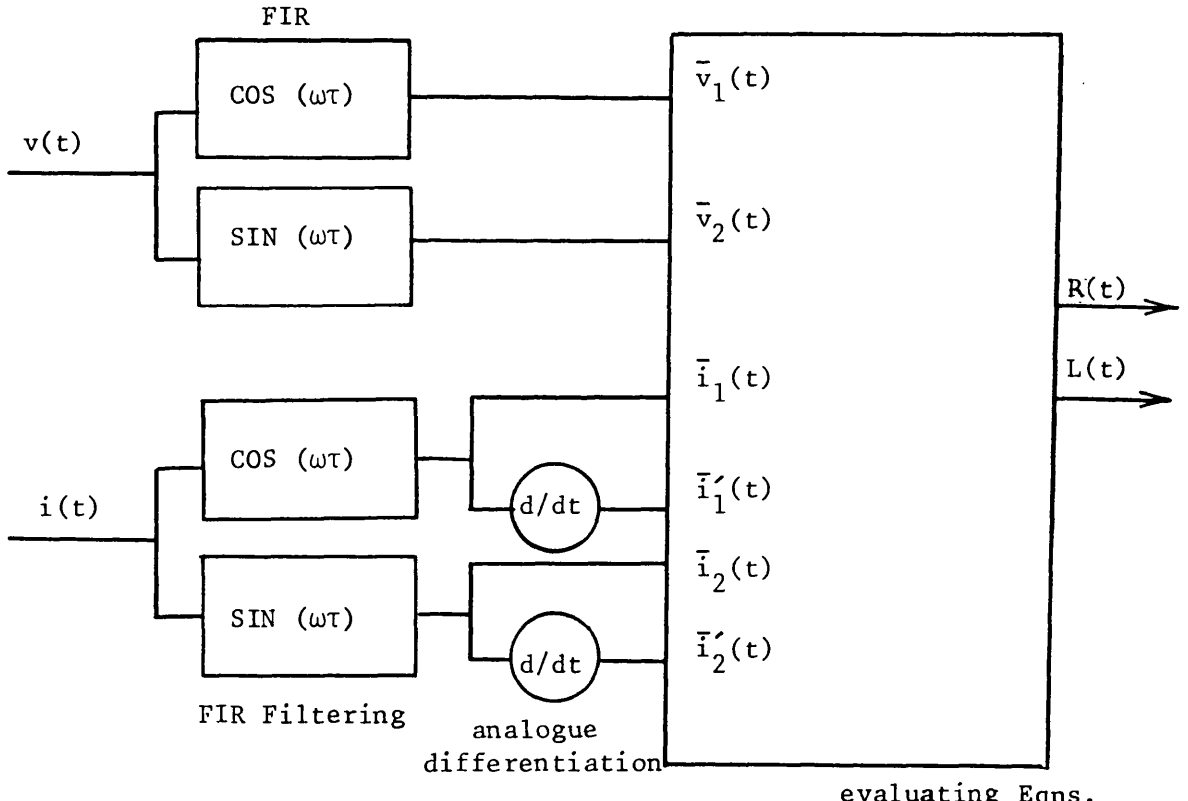


Fig. 4.2 : Time domain matrix solution

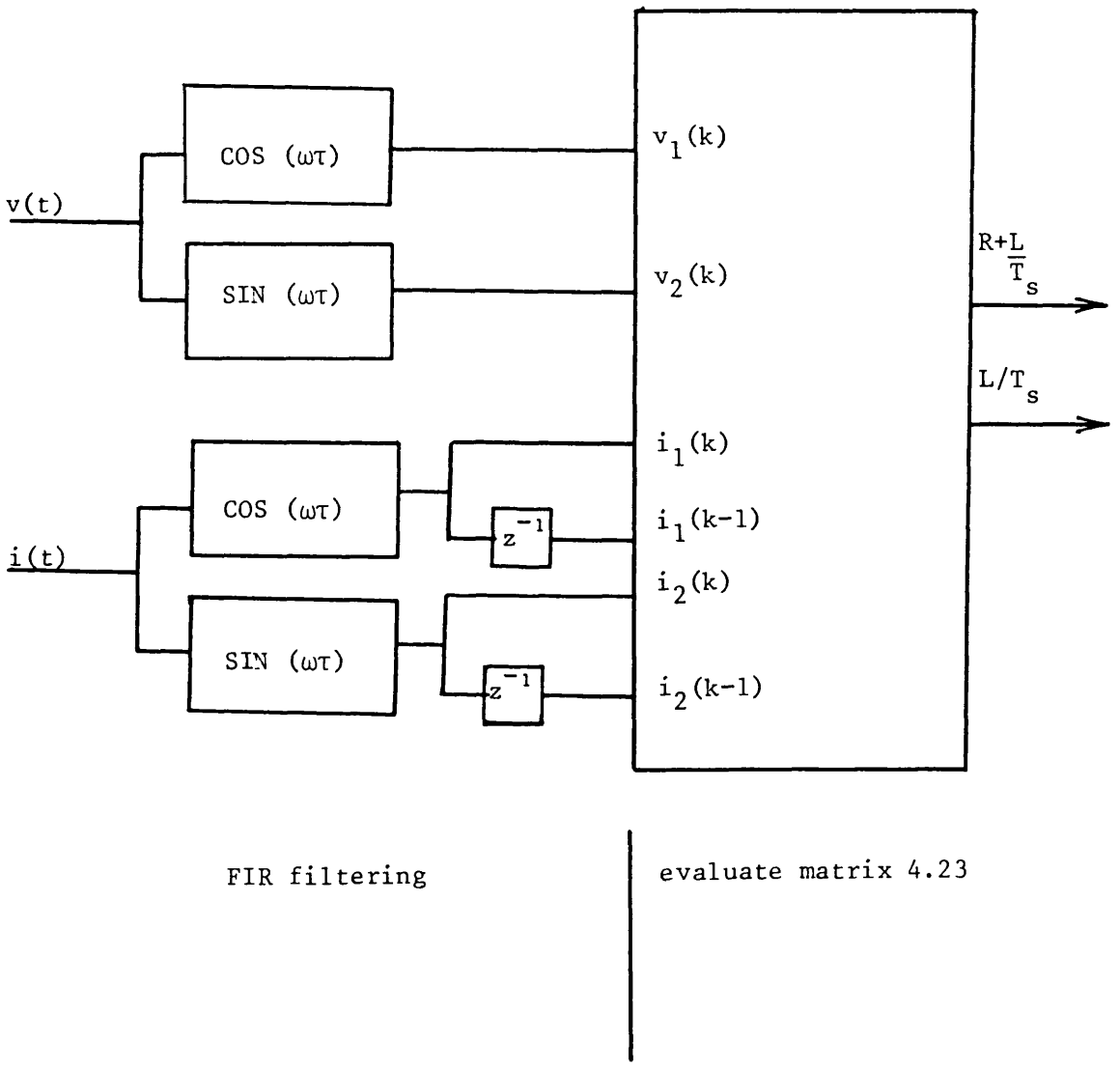


Fig. 4.3 : Discrete processing technique solution

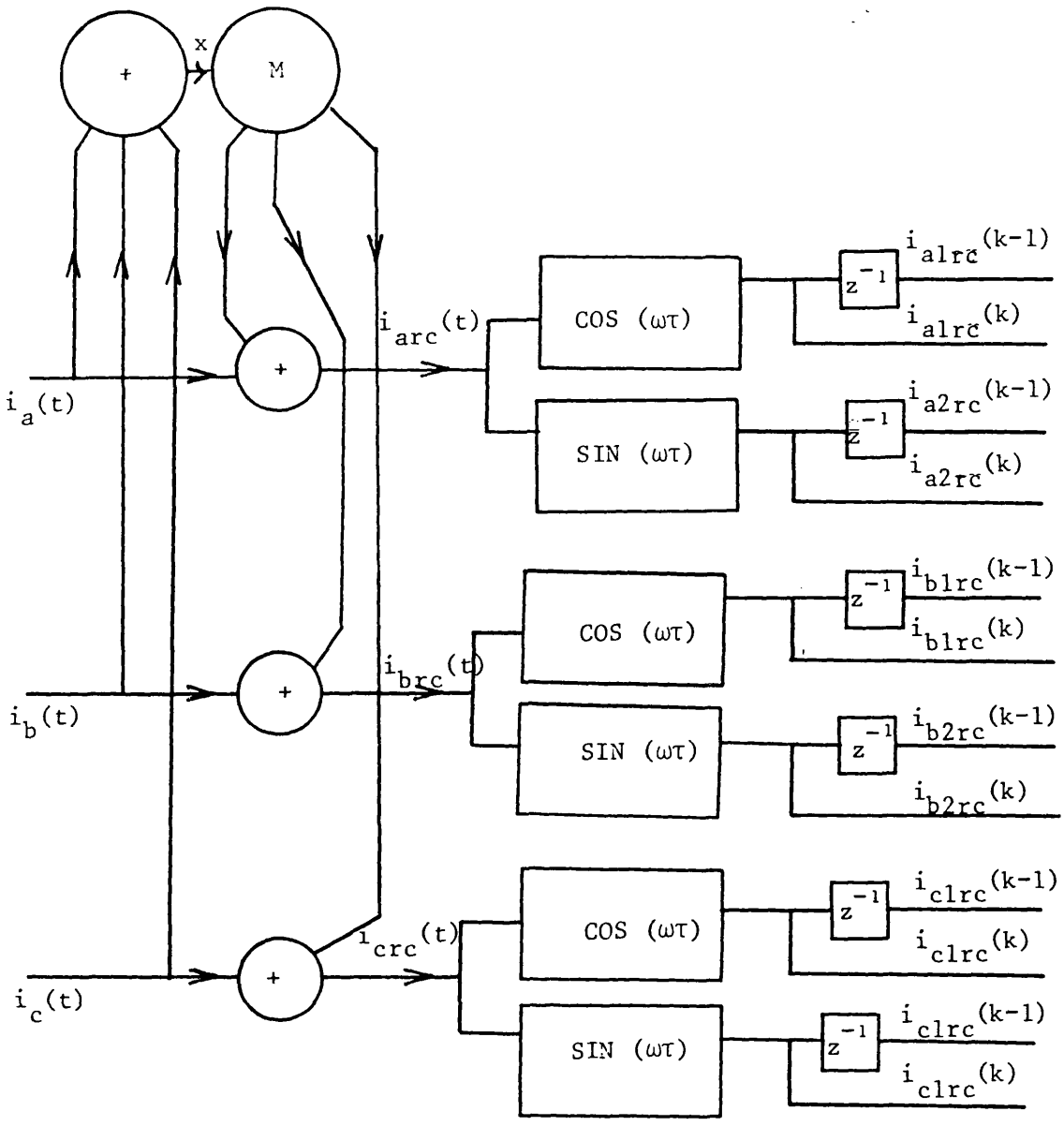


Fig. 4.4a : Relaying current signals formation

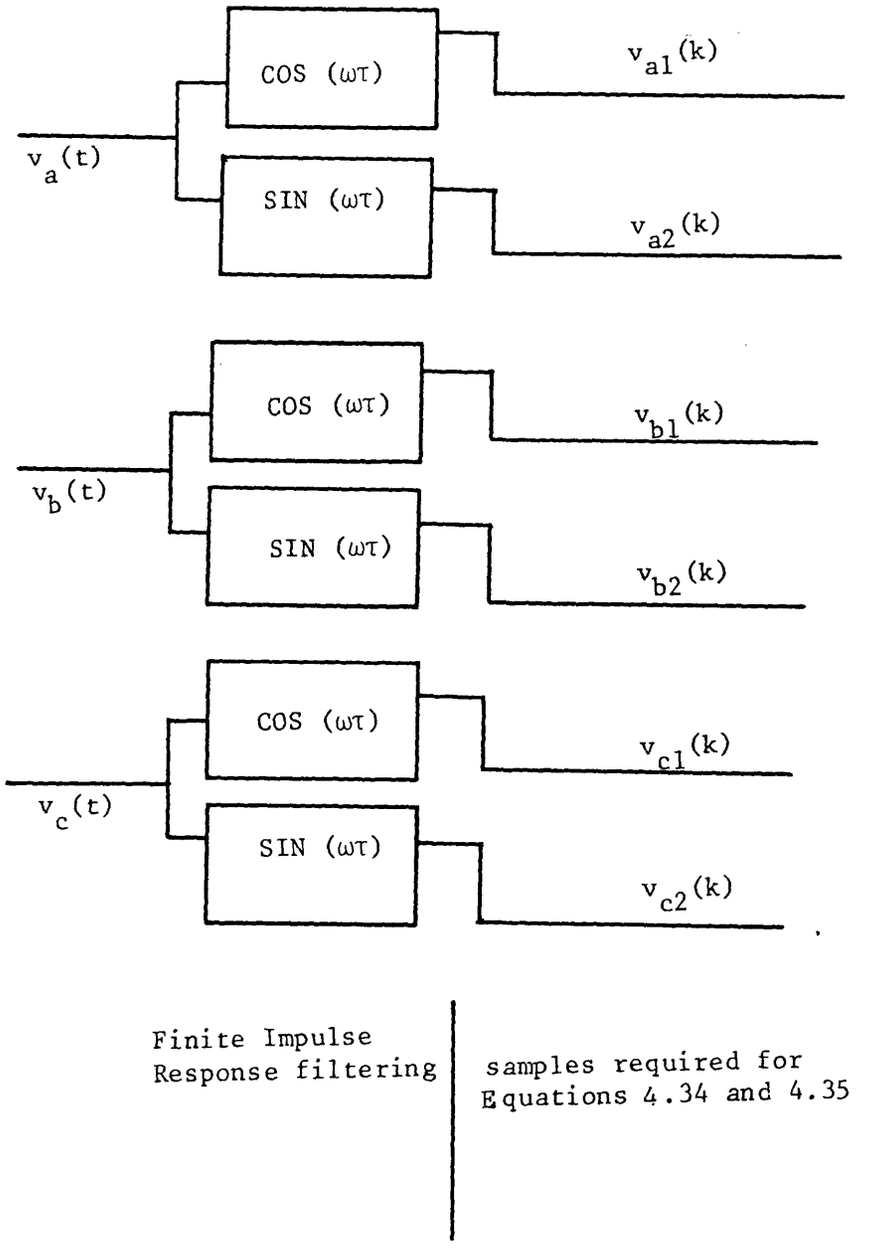


Fig. 4.4b : Relaying voltage signals formation

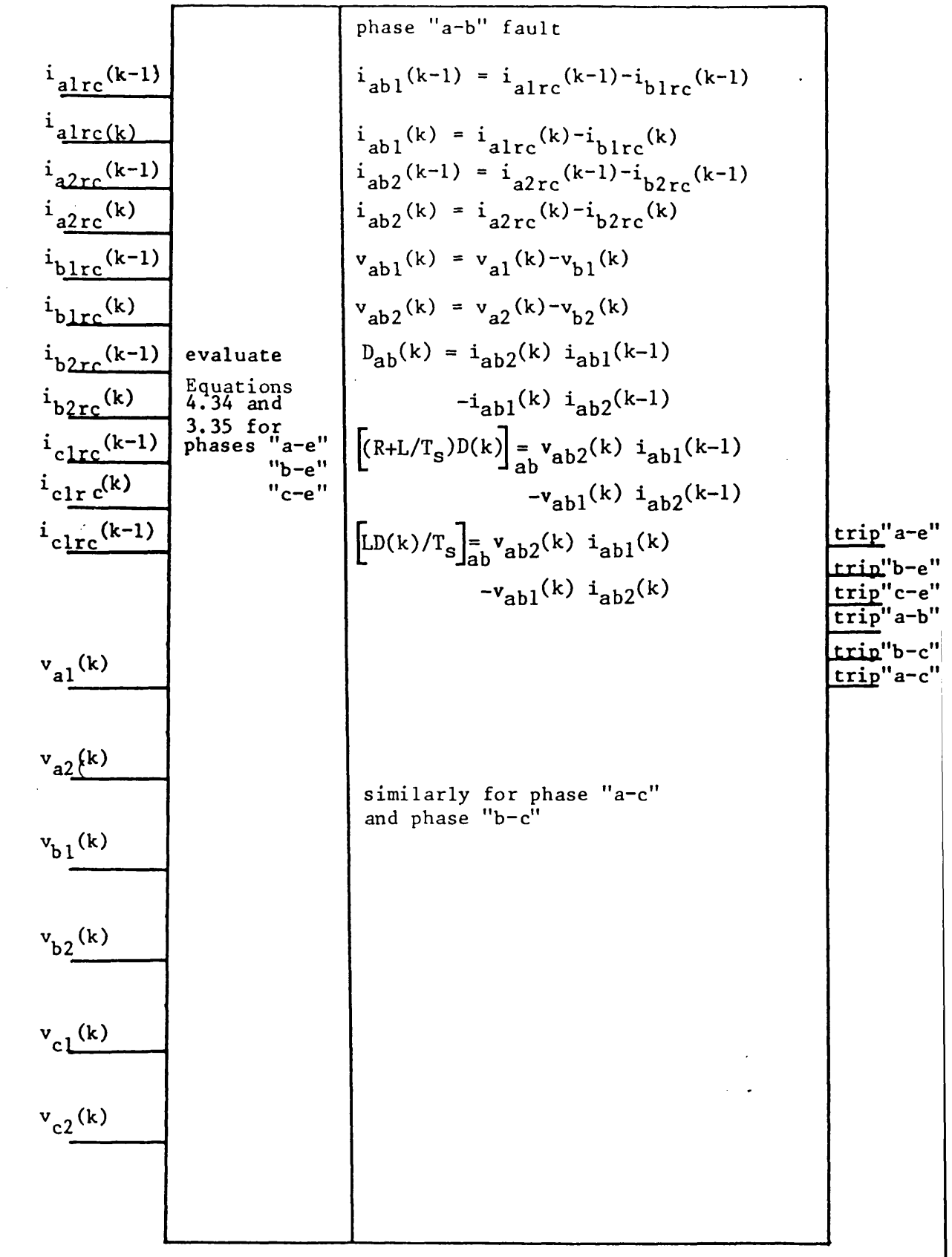


Fig. 4.4c : System data manipulation

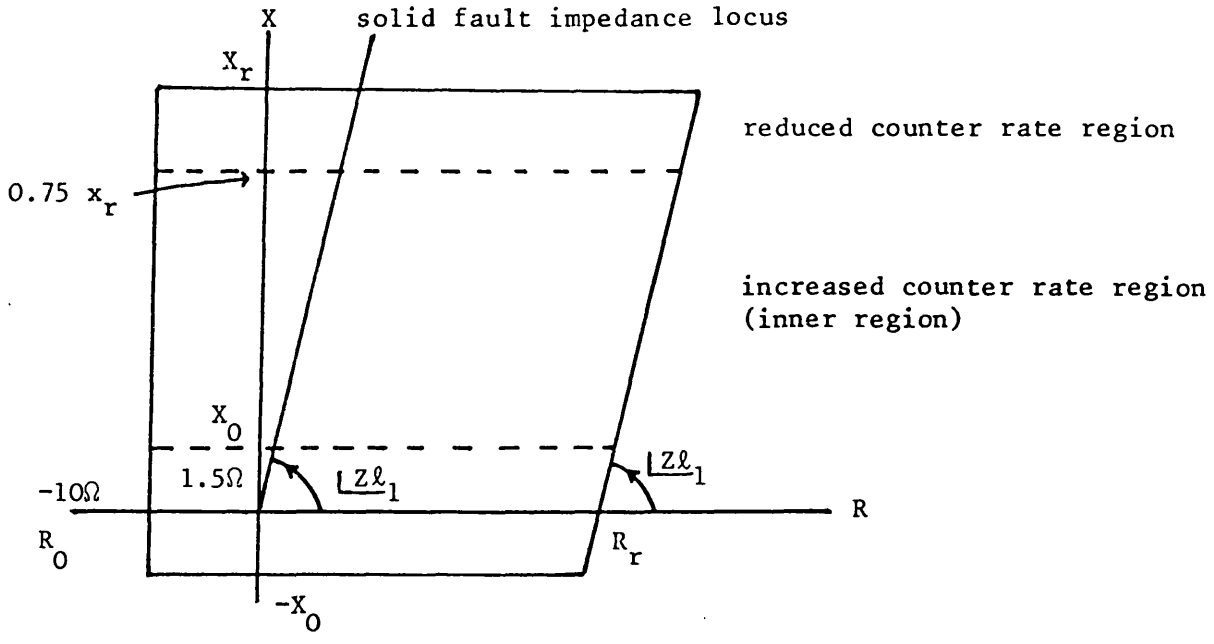


Fig. 4.5 : Quadrilateral tripping characteristic

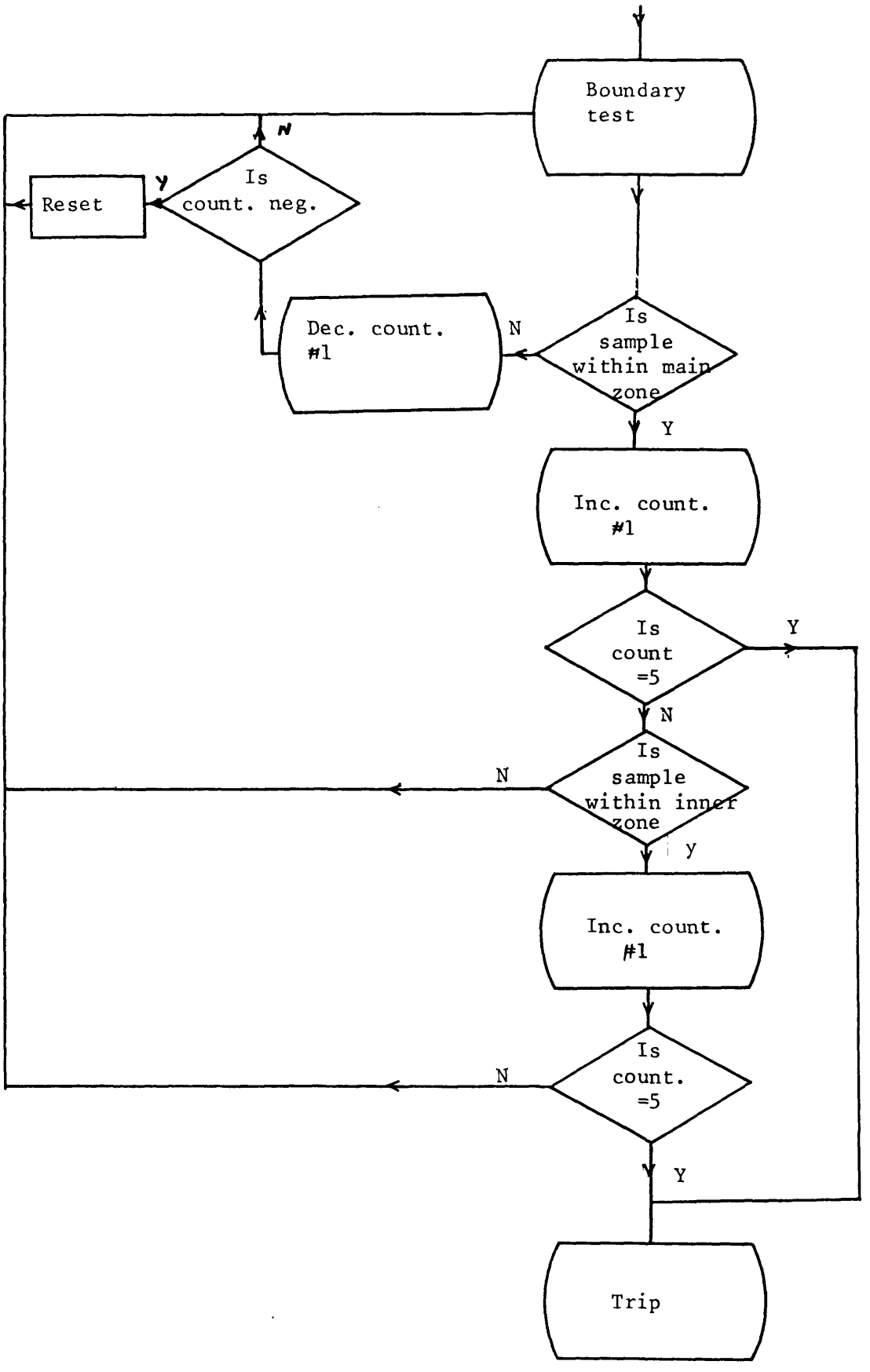


Fig. 4.6 : Decision logic process flow chart

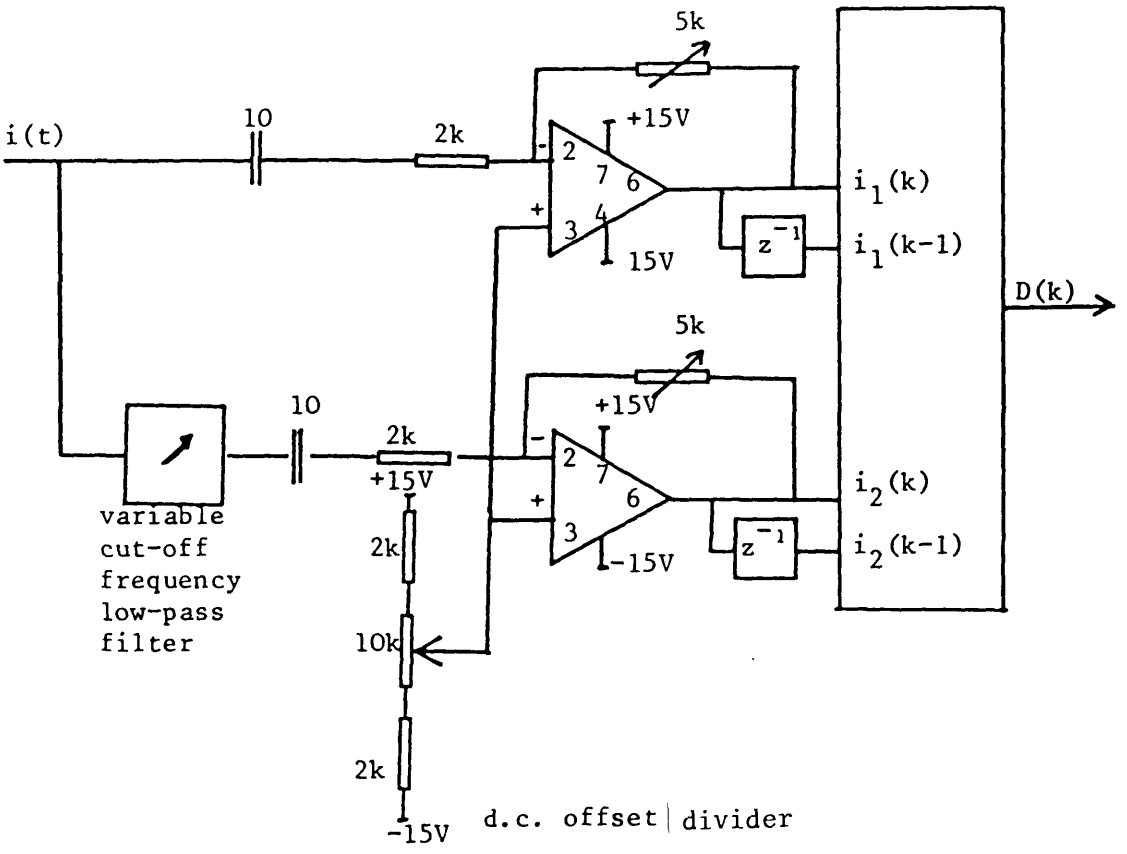


Fig. 4.7 : The behaviour of D(k) test circuit

All resistors are in Ω unless otherwise specified

All capacitors are in μF unless otherwise specified

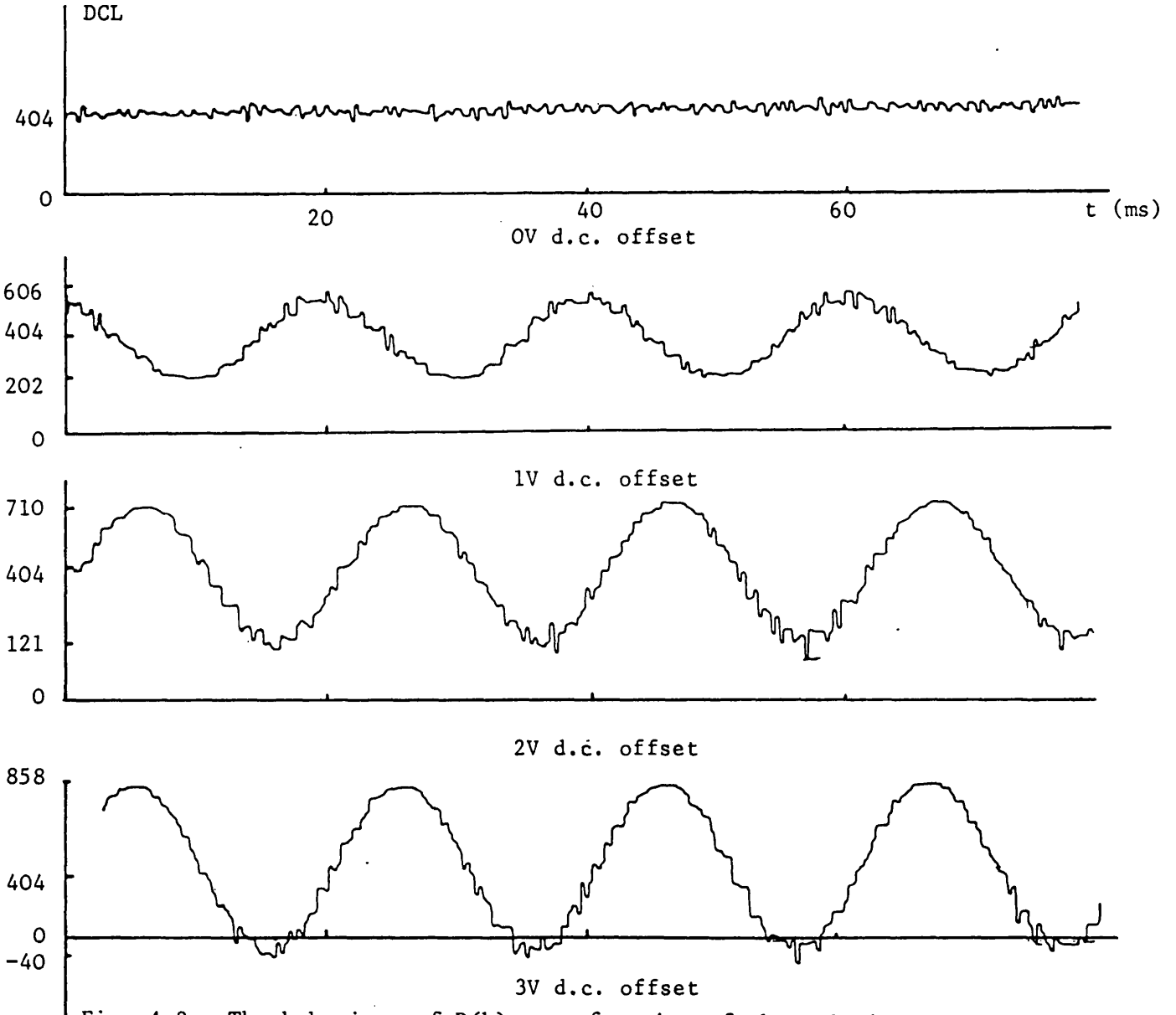


Fig. 4.8 : The behaviour of D(k) as a function of the relaying current exponential offset using 10 V sinusoidal input

CHAPTER 5

RELAY HARDWARE STRUCTURE

5.1 PROCESS ORGANISATION

The distance protection discrete solution requires implementation of Eqns. 4.34 and 4.35, which are given by:

$$K_3\ RD(k) < LD(k)/T_s < K_4\ D(k) \quad \text{--- 5.1}$$

$$R_0\ D(k) < RD(k) < R_r\ D(k) + K_5\ LD(k)/T_s \quad \text{--- 5.2}$$

where

$$D(k) = i_2(k)\ i_1(k-1) - i_1(k)\ i_2(k-1) \quad \text{--- 5.3}$$

$$(R+L/T_s)D(k) = v_2(k)\ i_1(k-1) - v_1(k)\ i_2(k-1) \quad \text{--- 5.4}$$

$$LD(k)/T_s = v_2(k)\ i_1(k) - v_1(k)\ i_2(k) \quad \text{--- 5.5}$$

$$RD(k) - (R+L/T_s)D(k) - LD(k)/T_s \quad \text{--- 5.6}$$

The numerical value of the constants K_3, K_4 and K_5 are given in Appendix 2.

The algorithm implementation can be represented as three distinctive operations. First, the extraction of the Fourier Transform components denoted by the subscripts 1 and 2 in Eqns. 5.3 to 5.5 which represent the real and imaginary terms of the transformed components of the relaying signals. Secondly, the manipulation of the filtered signals to establish $D(k)$, $(R+L/T_s)D(k)$, $LD(k)/T_s$ and $RD(k)$ as given by Eqns. 5.3 to 5.6. Thirdly, the implementation of the quadrilateral characteristic boundary test as given by Eqns. 5.1 and 5.2, using a

decision logic process as described in Section 4.3. Fig. 5.1 shows the process block diagram.

5.2 DISTANCE PROTECTION PRACTICAL CONSTRAINTS

The relay hardware structure must be capable of meeting the conventional distance protection accuracy, nominally 5% at the relay reach, and go further in achieving the advantage of speed and consistency of operation required for one-cycle fault clearance. For a finite transformation window, the post-fault impedance estimate is dictated by the transformation window width T_w and the sampling rate. The discrete process simulation showed that a sampling rate of 4 kHz is required for u.h.s. performance.

As described in Appendix 4, consideration must be given to the dynamic range of the signal processing scheme. In this respect it must be noted that the analogue components signal to noise ratio should exceed 60 dB and the digital process must have a resolution higher than 8-bit accuracy, since an 8-bit resolution will not exceed 48 dB.

5.3 THE FINITE FOURIER TRANSFORM COMPONENTS FORMATION

The finite Fourier Transform components are established by correlating a finite data window, with reference sine and cosine waveforms as given by:

$$v(t) = \int_0^{T_w} [COS(\omega\tau) + jSIN(\omega\tau)]\, v(t-\tau)\, d(\tau) = \int_0^{T_w} COS(\omega\tau)\, v(t-\tau)\, d(\tau) + j\int_0^{T_w} SIN(\omega\tau)\, v(t-\tau)\, d(\tau) \quad \text{--- 5.7}$$

$$v(t) = v_1(t) + jv_2(t) \qquad \text{--- 5.8}$$

The process function diagram is shown in Fig. 5.2. The process of establishing the transform components involves the convolution of the data window with the reference sine and cosine waveforms, which is equivalent to performing finite impulse response filtering (FIR) using sine and cosine filter impulse responses. In discrete form, the convolution process is represented by:

$$v(k) = h_0\, v(k) + h_1\, v(k-1) + \ldots h_n\, v(k-n) = \sum_{n=0}^{N-1} h_n\, v(k-n) \qquad \text{--- 5.9}$$

where the discrete variable k replaces the continuous time variable t, h_n are the filter impulse response coefficients and v(k-n) are the voltage samples within the finite time window. The cosine filter component $v_1(k)$, and the sine filter component $v_2(k)$, for "a" phase voltage are given by Eqns. 5.10 and 5.11 respectively:

$$v_{a1}(k) = h_{10}\, v_a(k) + h_{11}\, v_a(k-1) + \ldots h_{1n}\, v_a(k-n) \qquad \text{--- 5.10}$$

$$v_{a2}(k) = h_{20}\, v_a(k) + h_{21}\, v_a(k-2) + \ldots h_{2n}\, v_a(k-n) \qquad \text{--- 5.11}$$

where h_{1n} and h_{2n} are the cosine and sine reference waveform samples respectively.

In order to implement the finite Fourier Transform, each sample is fed into an N location shift register as shown in Fig. 5.3, which holds the sample history in time specified by the transformation window width T_w. As each new sample is entered into the first location of this register, all previous samples move one location to the right, and the sample in the Nth location is discarded. The elements of the shift register are multiplied with the reference sine and cosine filter coefficients. The

summation of these products represents the Fourier Transform components of a finite window T_w.

For a full three phase system, the distance protection scheme requires the three phase voltages and the three phase currents. Hence a total of 12 finite impulse response filters are needed, to provide filtered signals for the six types of fault measurements, (three phase-earth measurements, and three phase-phase measurements). In this respect it must be noted that the three phase-earth residual compensated signals can be used for the three phase-phase measurements as shown in Appendix 1.

5.4 FILTERED SIGNALS MANIPULATION AND DECISION PROCESS

The 12 filtered signals are manipulated, to establish $D(k)$, $(R+L/T_s)D(k)$, $RD(k)$ and $LD(k)/T_s$, as given by Eqns. 5.3 to 5.6. The process of establishing these terms requires six multiplications for each type of fault. The quadrilateral characteristic can be implemented using an intelligent hardware structure, a microcomputer, where all the multiplication by constants in Eqns. 5.1 and 5.2 can be performed using arithmetic shift software instructions as shown in Appendix 2.

5.5 PARALLEL PROCESSING HARDWARE REALIZATION

One possible hardware solution, for the full three phase line system, is to use six parallel microcomputers, to provide three phase-earth and three phase-phase measurements. Each processor performs the FIR filtering and the data manipulation required by the decision logic process, as shown in Fig. 5.4. The process demand for multiplication, and the speed in which available microcomputers perform multiplication made the distance protection, u.h.s. application not possible. For example, to

extract the Fourier Transform components, using 16 sample FIR filters, each processor requires the performance of 64 multiplications, which, using an estimated multiplication time of 20 μs for a typical 16-bit microprocessor gives a total estimated time of 1280 μs, or a sampling rate of less than 1 kHz. Moreover, the filtered data manipulation and decision logic process will further reduce the sampling rate to a few hundred Hz. The microcomputers multiplication capability could be enhanced by using a fast hardware multiplier. However, the use of one hardware multiplier to service the six processors requires a complicated bus exchange logic, and involves inevitable wait states for the multiplier access. Alternatively, more than one hardware multiplier can be used to service the six processors, but the hardware structure will not be economically viable.

5.6 EXTERNAL FIR FILTERING AND ALTERNATIVE RELAY STRUCTURE

Early in the research, the six parallel processor scheme was abandoned and it was concluded that, the finite Fourier Transforms were to be performed externally, using existing FIR filtering technology, in order to reduce the processing burden on the processor unit.

As an alternative, a conventional hardware structure has been considered, consisting of external FIR filters and a processor unit. To establish the terms $D(k)$, $(R+L/T_s)D(k)$, $LD(k)/T_s$ and $RD(k)$, as given by Eqns. 5.3, 5.4 and 5.6, six multiplications are required for each type of fault, and the processor multiplying capability is enhanced using a hardware multiplier.

5.7 DISTANCE PROTECTION CONVENTIONAL HARDWARE STRUCTURE

In order to meet the sampling rate required for u.h.s. operation, a conventional hardware structure has been considered. The hardware structure consists of a data acquisition unit comprising the external FIR filters, a 16-bit microcomputer, and a multiplier unit incorporating a fast multiplier chip, to enhance the processor multiplying capability. Fig. 5.5 shows the relay hardware structure block diagram.

5.7.1 Data acquisition unit

Fig. 5.6 shows the data acquisition unit block diagram. In order to implement the finite transform algorithm, for full three phase systems, the relay requires the three phase voltages and the three phase currents, to extract the Fourier Transform components of a finite window. As mentioned previously, 12 FIR filters are needed, each clocked at 4 kHz as shown in Fig. 5.6. The filtered outputs are tracked using sample and hold circuits, clocked at 4 kHz. The analogue filtered signals are converted to 12-bit long words, since it has been found that the 12-bit resolution is adequate to meet the process accuracy. The use of 12 analogue-to-digital (A/D) converters is considered uneconomical and in preference an analogue multiplexer scanned at 64 kHz is used.

Data transfer to a microcomputer using interrupts is not convenient for real-time signal processing, since during the interrupt acknowledgement, the processor must save the program counter and status, which is time consuming. Alternatively, the converted data set, consisting of six transformed voltage components and six transformed current components can be stored in external memory and transferred through a parallel input-output port PIA at the start of each processing cycle (250 μs for

4 kHz sampling rate). However, conventional microcomputers are provided with 8-bit parallel ports and each word (16 bits) has to be transferred as two bytes. Moreover, the data transfers to the processor memory using the PIA have to be routed through one of the central processing unit (CPU) registers. For a fast microcomputer, with a byte transfer time of 2 μs, the overall time for a word transfer is 8 μs plus the destination address calculation, which gives a total transfer time of approximately 12 μs. For a three phase system, a total time of 144 μs is required to transfer the 12 voltage and current components. The consumption of 144 μs on data transfer, for a demanding real-time u.h.s. application, where a high sampling rate is required, is not acceptable, and a more advanced technique, direct memory access (DMA) must be used.

5.7.2 Processor unit

The data manipulation, the quadrilateral characteristic boundary testing and the decision logic process requires the use of a microcomputer. Since an 8-bit processor resolution does not exceed 48 dB as described in Appendix 4, and that is below the required process accuracy, a higher resolution process has to be used. The processor must be a fast 16-bit microcomputer, complete with memory required by the scheme, control circuits and service facilities. At the start of this research work four 16-bit microcomputers were available: Texas TM9900, Intel MCS8086, Zilog Z8002 and Motorola M68000. The choice of the appropriate microcomputer was governed by two factors, the machine speed, and the machine availability. The theoretical bench mark studies revealed that the Texas TM9900 was the slowest among the available processors and it was discarded. The M68000 was available in development version only and it was consequently discarded. The Intel MCS8086 and the Zilog Z8002 had

an identical bus structure. The Z8000 possessed a speed advantage and was therefore chosen. The Z8000 family of processors are available in two versions, Z8001 and Z8002. The Z8001 is a segmented version, with 23 address bits, capable of addressing an 8 Mbyte of memory. This is far in excess of that required for the algorithm implementation. The Z8002 is a non-segmented version with a 16-bit address bus, capable of addressing 65 kbyte of memory. The latter is more appropriate for the relay development. These considerations at the start of the research led to the choice of the Z8002 processor.

5.7.3 Multiplier unit (MU)

The discrete process algorithm, for the six types of fault measurements (Eqns. 5.3 to 5.5), requires 36 multiplications. The available microcomputers perform the multiplication process in a relatively longer time compared with hardware multipliers. Investigation has shown that it is not possible to use the multiply software instruction and at the same time maintain a 4 kHz sampling rate. For example the Z8002 microcomputer, multiplies two 16-bit binary operands to produce a 32-bit product in 20 μs. Thus the time required to evaluate Eqns. 5.3 to 5.5, for the six types of faults is 720 μs. This represents approximately 300% of the available processing time: 250 μs. At this stage it is essential to use a fast hardware multiplier, in order to meet the 4 kHz sampling rate. The multiplier unit is based on a fast 16-bit multiplier chip. The multiplier unit, multiplies two 16-bit binary vectors and produces a third vector from the product of the first two.

A 16-bit data transfer through the microcomputer PIA takes 12 μs, as described in Section 5.7.1. For the multiplier unit data transfers,

which involves the transfers to/from the processor memory of 108 words, with total time of 1296 μs for the six types of fault measurement and this represents 518% of the available CPU time. In order to reduce the data transfer time and to improve the throughput rate to the multiplier chip, a DMA technique must be used. Fig. 5.7 shows the hardware structure block diagram.

5.8 SYSTEM DATA PIPELINING

In order to achieve the 4 kHz sampling rate for a full protection scheme, a pipelining technique has been considered. The pipeline technique incorporates two sets of data processed concurrently by the multiplier unit and the processor unit, as shown in Fig. 5.8. The initial estimation of the overall process time for the six types of fault is 426 μs, which implies the use of at least two Z8002 microcomputers.

For development purposes, a single phase to earth fault measurement is implemented, where the data pipelining is shown in Fig. 5.9. The initial estimation time for a single phase to earth fault is 250 μs. The multiplier unit buffer access is reduced to one, since the quadrilateral characteristic boundary test can be performed through the Z8002 CPU arithmetic shift instructions shown in Appendix 2.

5.9 TEST UTILITY

The investigation of the discrete process solution, requires access to different terms of the algorithm. The access to the digital process in binary form, does not give an overall picture regarding the relay performance. In the course of the relay hardware testing, it is essential to provide tests under software control, for rapid hardware fault

diagnostics. To meet these two requirements, a fast 12-bit digital-to-analogue converter (D/A) has been proposed.

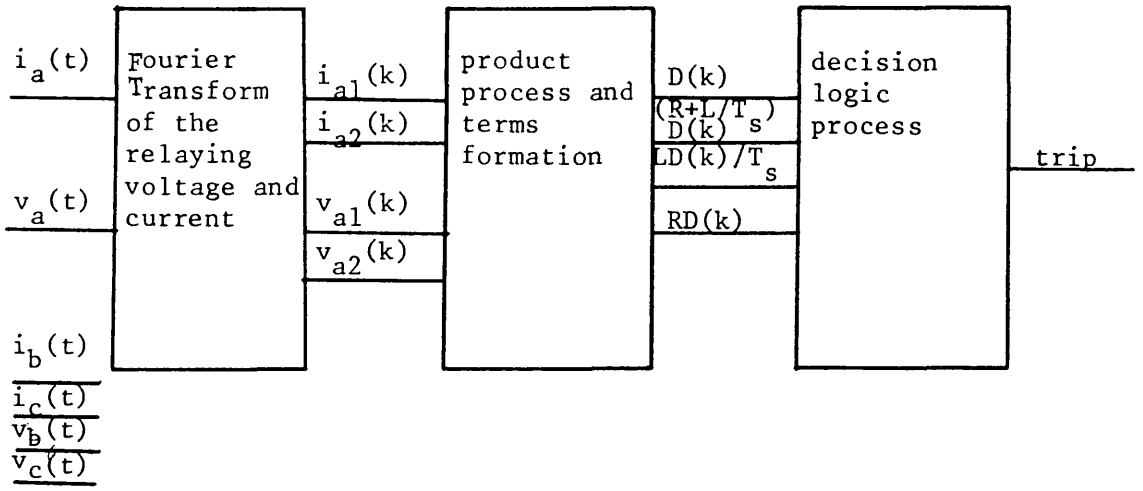


Fig. 5.1 : Process functional description

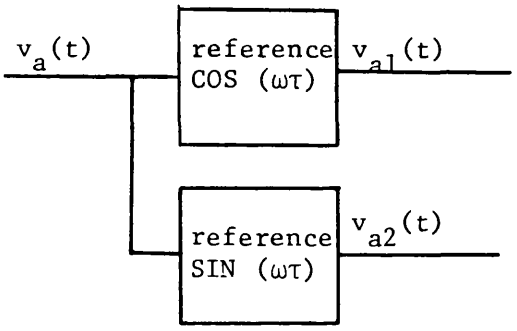


Fig. 5.2 : Fourier Transform process block diagram

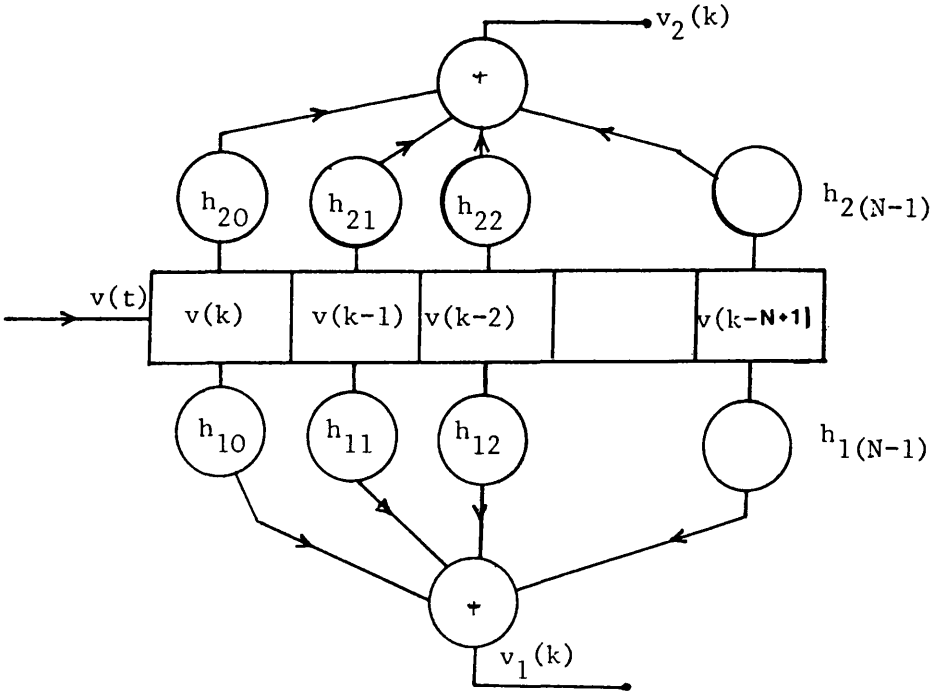


Fig. 5.3 : FIR filter block diagram

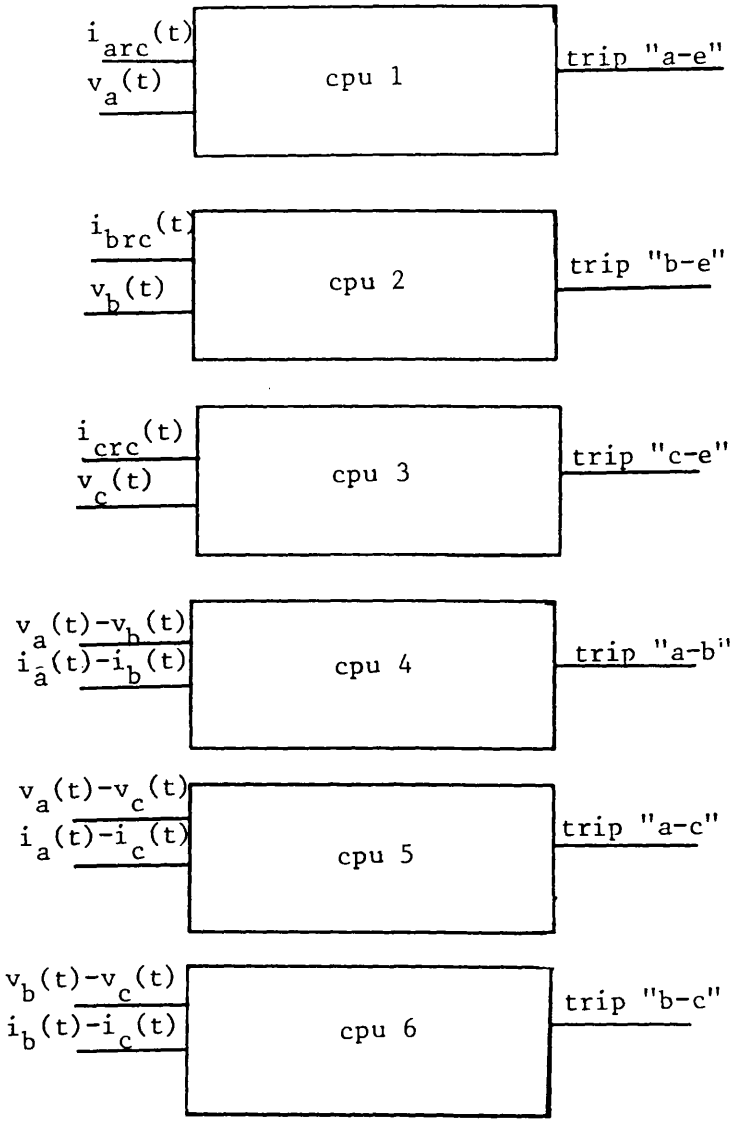


Fig. 5.4 : Full 3-phase scheme hardware structure using six parallel processors

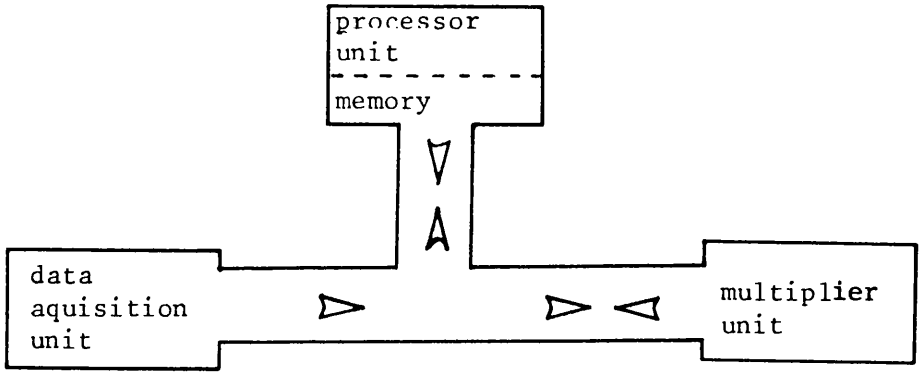


Fig. 5.5 : Conventional hardware structure block diagram

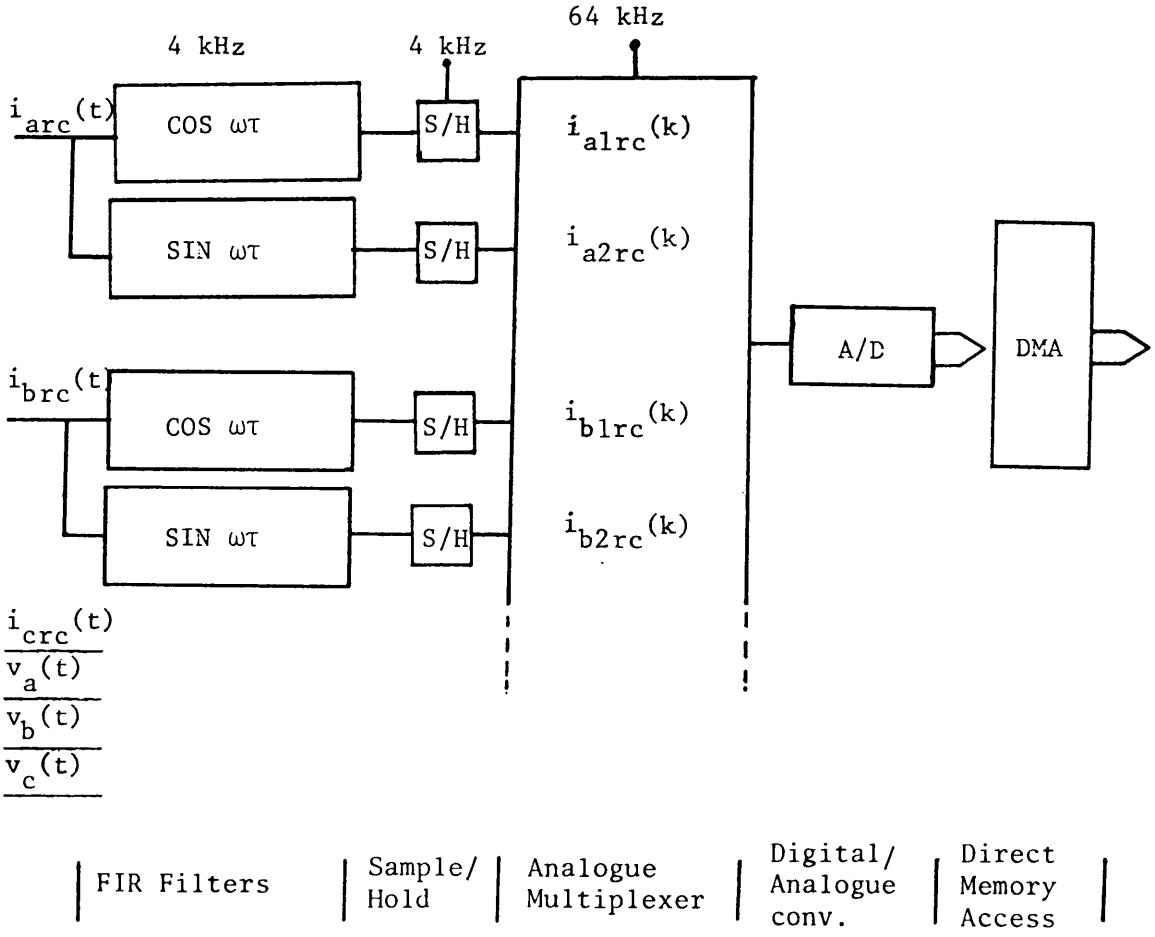


Fig. 5.6 : Data acquisition unit block diagram

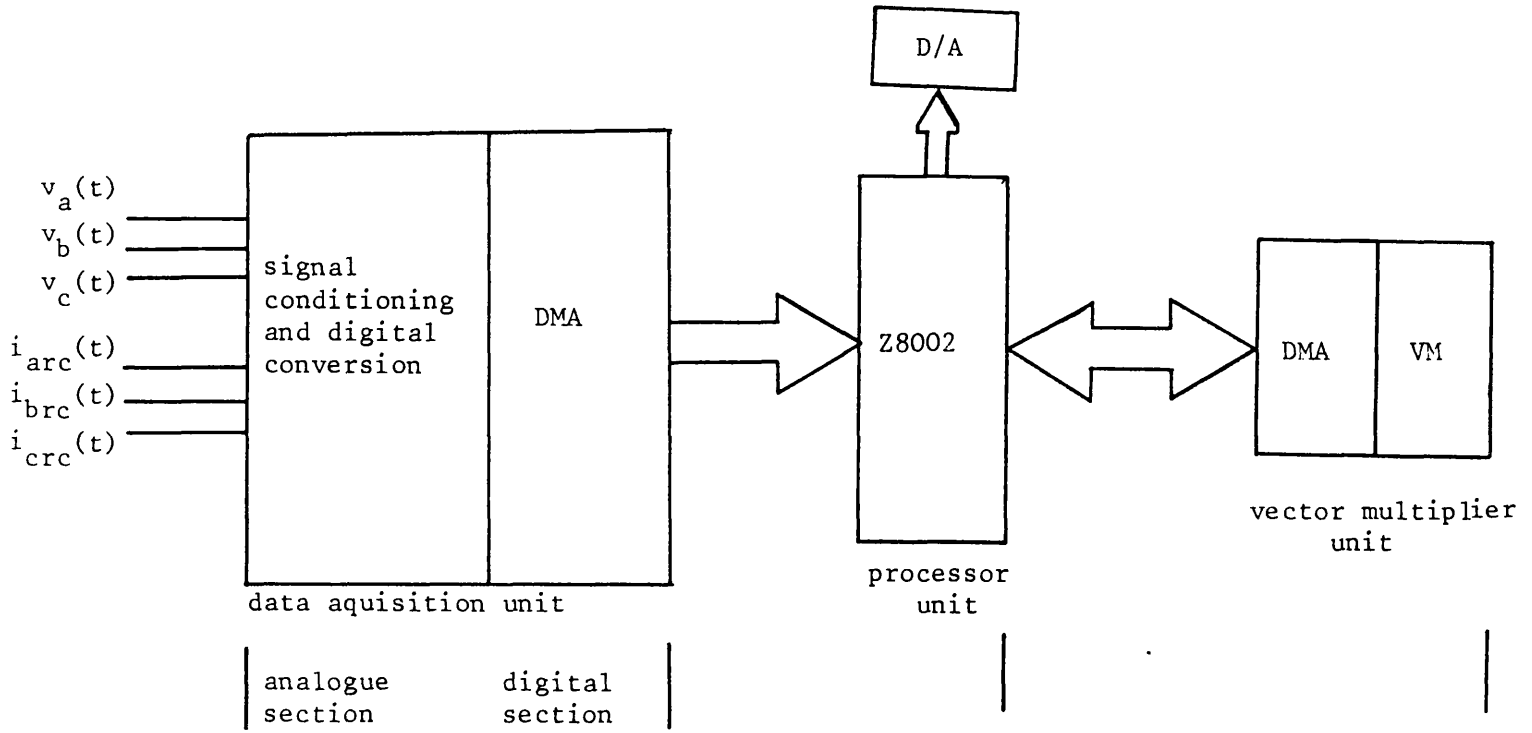


Fig. 5.7 : Relay hardware structure block diagram

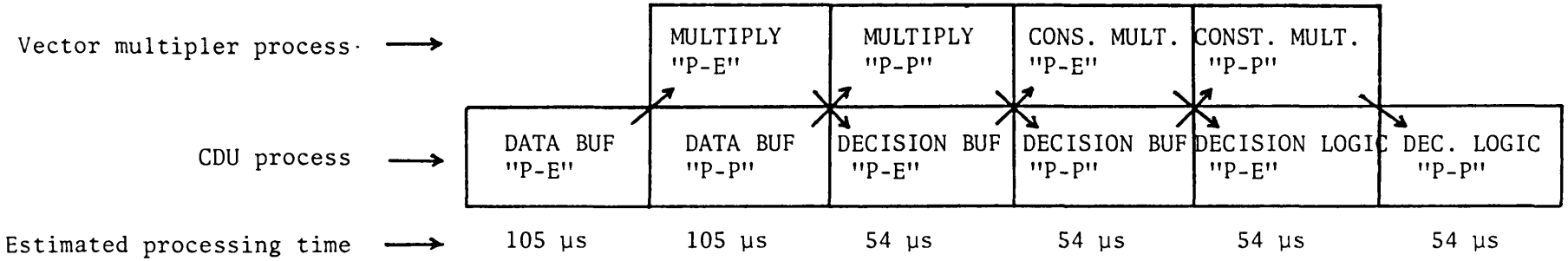


Fig. 5.8 : Data pipelining for the 6-types of fault
where "P-E" is for phase-earth fault
and "P-P" is for phase-phase fault

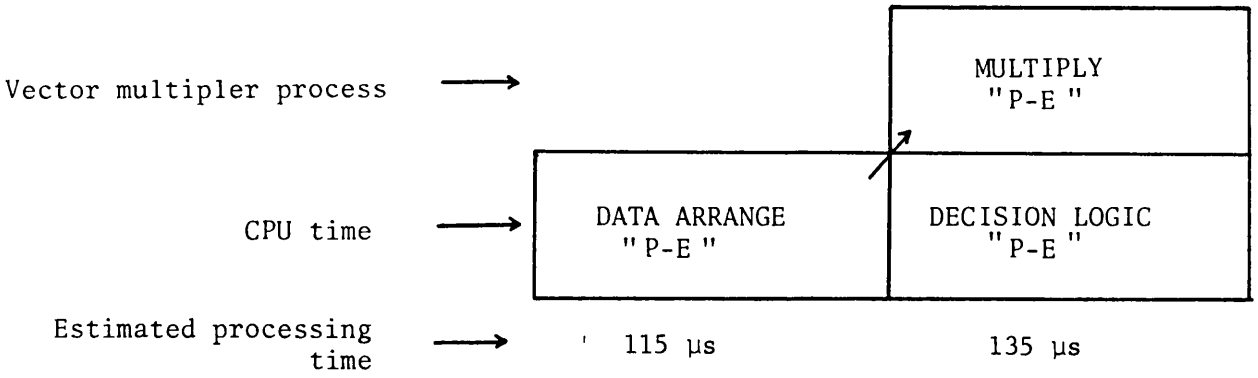


Fig. 5.9 : Single phase-earth data pipelining

CHAPTER 6

PROCESSOR AND MULTIPLIER UNIT

6.1 INTRODUCTION

As described in Chapter 5, the evaluation of the discrete solution, requires the manipulation of the filtered signals which can be achieved using a microcomputer with enhanced multiplication capability. The microcomputer unit must be provided with service and interface facilities. These services are provided through the 4116 monoboard microcomputer, based on Z8002 CPU.

6.2 PROCESSOR BOARD FUNCTIONAL DESCRIPTION

The 4116 monoboard microcomputer (MBM) contains a Z8002 CPU, two serial communication ports, a timer controller, an interrupt controller and a parallel interface adaptor, as shown in Fig. 6.1.

The Z8002 CPU is a programmable 16-bit chip, capable of accessing 64 kbyte of internal memory. The 4116 MBM is provided with 32 kbyte of dual-port random access memory (RAM), required for the data manipulation and software development. The RAM can be accessed simultaneously from peripherals and the CPU. Access arbitration for two port operation provides 50% interleave of Z8002 CPU and a peripheral access. Control defaults to the Z8002 if no peripherals requests are active.

The 4116 MBM contains a programmable peripheral interface adaptor (PIA), which consists of three parallel input/output ports, two 8-bit bidirectional data ports and the third port is configured as two 4-bit ports, to provide control lines for the two 8-bit ports. Any of the control

port bits can be set or reset by the CPU, thereby providing handshake signals for parallel data communication.

Two serial communication interface devices are provided for the 4116 board, one for a VDU interface and the second for a printer interface.

The monoboard microcomputer is provided with a programmable interrupt controller, capable of resolving the priority of eight interrupt levels. A higher priority input will interrupt a lower priority interrupt from being serviced. A lower priority interrupt will be held for later service.

The system includes a system timer controller (STC), to provide facilities for counting and timing operations. The STC is capable of providing waveforms of various duty cycles, as required for the application.

6.3 Z8002 DOWNLOAD

The 4116 monoboard system is provided with a monitor program, which on power-up initialize the board components and provides communication facilities. The ROM-base monitor also provides facilities for examining and substituting the system memory. Although most modern microcomputer monitors are provided with download facilities from a host computer, the 4116 MBM monitor is not. For the purpose of relay software development, a download program was written for running on the host computer (PDP 11/23). The Z8002 download technical description is given in Appendix 5, Section A5.1.

6.4 4116 MBM BUS STRUCTURE

For microcomputer systems, there are two factors which govern their capability; speed and bus structure. The data highway or bus carries the necessary signals to allow various system modules to interact with each other. The 4116 system uses the Intel Multibus structure [22]. The Multibus structure is based on a master-slave concept. A master device is a module which has the ability to control the bus, and the master exercises this control by acquiring the bus through the bus exchange logic. A bus slave is a device addressed by the bus master, and acts upon its command signals. The slave is not capable of controlling the Multibus interface. The Multibus exchange signals and bus exchange unit are described in Appendix 5, Sections A5.2 and A5.3.

6.5 MULTIPLIER UNIT

As described in Section 5.7.3, the evaluation of the terms D(k), LD(k) and RD(k), for a scheme incorporating the six types of fault, requires 36 multiplications. In order to meet the u.h.s. performance, which requires a sampling rate of 4 kHz, the microcomputer multiplication capability must be enhanced using a fast hardware multiplier chip (TRW-MPY 16). The data transfers to and from the multiplier are performed using a DMA technique. The multiplier chip, Fig. 6.2, is a high speed 16-bit multiplier, which multiplies two 16-bit binary numbers (X and Y) and generates a 32-bit product (P). The product P becomes available, typically 100 ns following the latch of the Y multiplicant to its corresponding register. As the product becomes available, it can be latched to the input of the product tri-state buffer, using CLKM and CLKL signals (M and L are references to the most and least significant words of the product). The product is released by enabling

the tri-state output buffer, using the multiplier signals TRIM and TRIL.

6.5.1 Vector multiplier (VM) realization

One way of realizing the multiplier unit is to perform the multiplicants and the product transfers from fixed memory locations. The disadvantage of this technique is that the processor must enable the multiplier unit DMA prior to a multiplication, which adds 2 μs for each multiplication.

In order to utilize the multiplier unit efficiently, the multiplicants can be arranged in a data buffer and accessed sequentially by the DMA unit. The products are returned to a second buffer. This can be achieved by programming the DMA transfer parameters, source and destination vector addresses and string length. The technical description of the vector multiplier unit is given in Appendix 5, Section A5.4.

6.6. SYSTEM TIMER CONTROLLER (STC)

As described in Chapter 5, the relay hardware requires various timing waveforms, in order to maintain the discrete process synchronous integrity. It will be shown in Chapter 7 that the relay requires 64 kHz, 16 kHz, 4 kHz and 2 kHz 50% duty cycle waveforms and 4 kHz and 2 kHz short duration reset pulses. The required timing signals are generated by the programmable (STC). The STC is a support device for processor oriented systems, and enhances the system capability with respect to counting and timing operations. The STC contains an internal oscillator and associated frequency scaling circuitry plus five general purpose 16-bit counters. Each counter is supported by control circuitry that allows it to be independently configured for the required task. The STC features and programming are given in Appendix 5, Section A5.5.

6.7 D/A CONVERTER UNIT

As described in Section 5.9, the investigation of the discrete process solution requires the use of a D/A converter. The D/A converter used (DAC 80) is a 12-bit converter, which converts 12-bit digital data to an analogue signal in 5 μs. The D/A converter memory mapping and circuit description are given in Appendix 5, Section A5.6.

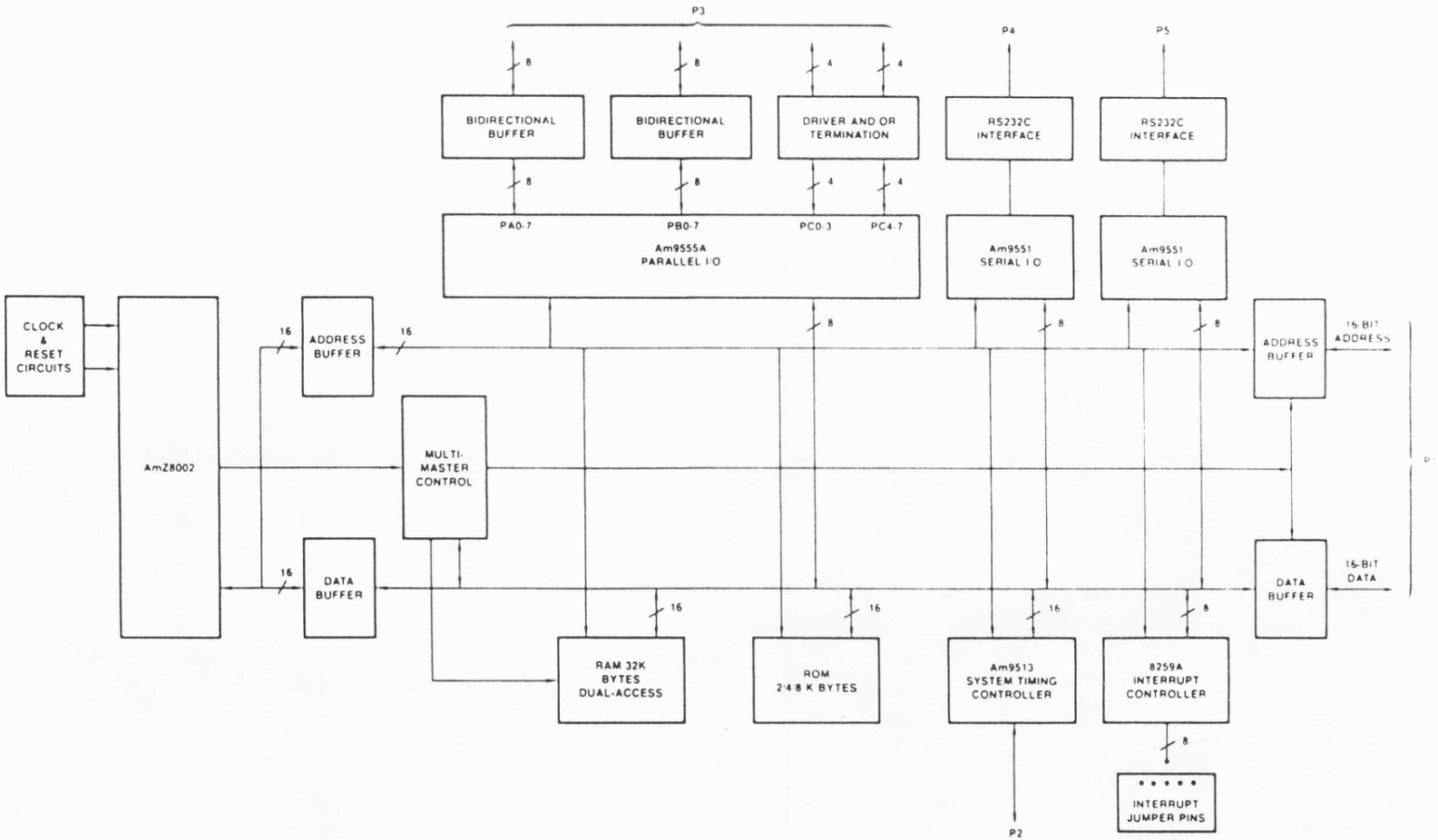
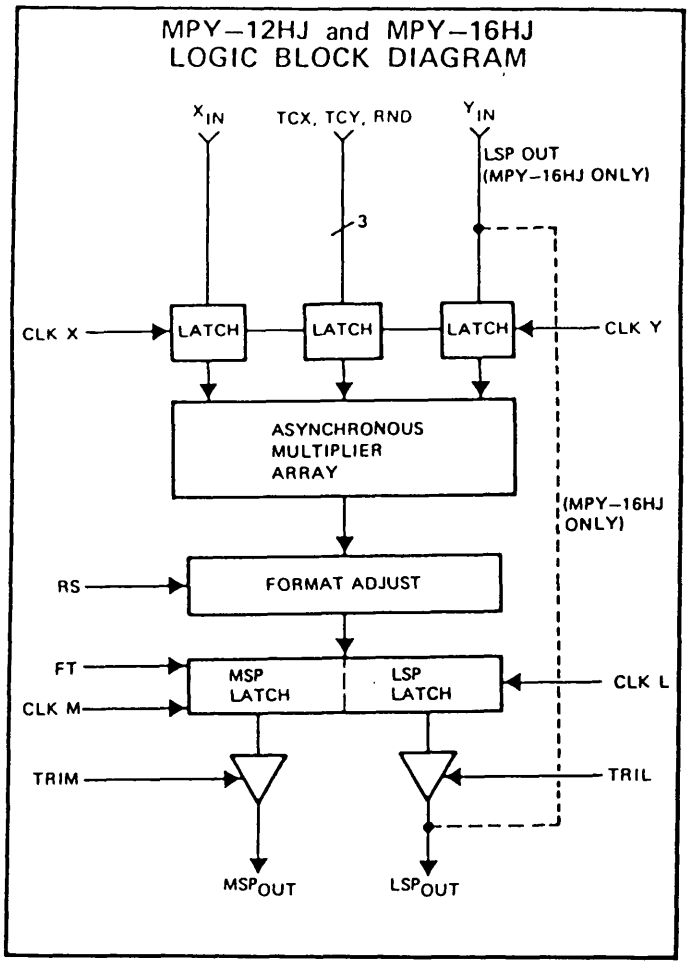


Fig. 6.1 : 4116 monoboard microcomputer block diagram



CONTROLS

(Positive logic unless otherwise noted)

CLK X – X_{IN} Register Clock

CLK Y – Y_{IN} Register Clock

CLK L – LSP Register Clock

CLK M – MSP Register Clock

TRIL – LSP Three-State Control,
TRIM – MSP Three-State Control,
RS – Right Shift MSP word down 1 bit, removes LSP SIGN bit.
FT (Feedthrough) – Makes output latch transparent

TCX, TCY – Denotes respective input words as two's complement (logic 1) or magnitude (logic 0) data format (registered control inputs strobed by respective clocks)

ROUND – ADDS 1 to MSB bit of LSP word, regardless of shift position (registered control input strobed by [CLK X or CLK Y]).

Fig. 6.2 : TRW multipler chip architecture

CHAPTER 7

DATA ACQUISITION UNIT

7.1 DATA ACQUISITION UNIT STRUCTURE

As described in Chapter 5, the data acquisition unit consists of FIR filters, an analogue multiplexer, an analogue-to-digital converter and a direct memory access unit (DMA). The evaluation of the discrete solution expressed by Eqns. 4.34 and 4.35, requires the extraction of the Fourier Transform components, using FIR filters and the technique described in Section 5.2. The FIR filters have two functions, to extract the Fourier Transform components and to filter unwanted components from the relaying signals. The filtered signals are multiplexed via an analogue multiplexer and converted to 12-bit words. The converted data being transferred to the processor unit via a DMA process.

7.2 FIR FILTER REALIZATION USING CCD DEVICES

In order to realize a transversal (FIR) filter, an N-stage shift register is employed, to hold the samples history for a finite window width T_w, as shown in Fig. 7.1. The elements of the register are shifted one location to the right at intervals of T_s in time. The contents of the shift register are multiplied by the filter coefficients, which determine the filtering function. The sum of the products give the filter output. The filter output Y(k) is related to the input sequence by Eqn. 7.1:

$$Y(k) = \sum_{n=0}^{N-1} h(n)\ X(k-n) \qquad \text{--- } 7.1$$

where X(k-n) are the sampled inputs of the filter at intervals T_s seconds and h(n) are the filter coefficients. Fig. 7.1 shows the realization of the FIR filter.

In order to realize the required FIR filtering functions, use has been made of charge-coupled-device (CCD) tapped delay lines. One of the powerful concepts in CCD devices is a single chip easily realizing transversal filters. The CCD analogue processing technique is based on continuous sampling of variable data. The input signal is converted into discrete packets of charge, and clocked through the filter stages at uniform time intervals T_s. The CCD tapped delay lines permits the storage of analogue signals, which can be non-destructively sensed at successive delay times. The output from each tap is multiplied by a filter coefficient and the sum of these products gives the filter output. A Reticon TAD-32 CCD chip, which is 32 stage device, has been chosen to perform the FIR filtering of the relaying signals.

7.3 TAD-32 TAPPED DELAY LINES DEVICE

TAD-32 is a 32-stage charge-transfer-device, which permits the storage of an analogue signal. Each stage is tapped and brought to the outside through a buffer amplifier, thus allowing the filter stages to be sensed non-destructively at successive delays and permitting variable loading of taps, to create various tap coefficients. Appendix 6, Sections A6.1 and A6.2 gives the TAD-32 operation and drive circuit description.

7.3.1 FIR Filter realization using CCD devices

In realizing a transversal filter, a set of tap weights are selected in the discrete-time domain, to achieve the required filtering function. The filter coefficients are adjusted using a potentiometer for each tap. For the realization of the required filtering function, using a TAD-32, it is important that an active tap sees a low impedance, because a

potential variation at the tap affects the charge packet transfer to the next stage. The effect of taps loading can be clearly seen in Fig. 7.2, where 1 kΩ resistors are used, to preserve linearity. As the tap loading increases to 10 kΩ, excessive cross-talk was observed. The restriction of using low tap loads makes the use of a simple summing structure, such as virtual earth summing amplifier Fig. 7.3, impossible. The functional description of the summing amplifier shown in Fig. 7.3 is given by:

$$vo(t) = R2/R1\ [v1(t) + v2(t) + \ldots + vn(t)] \qquad \text{--- } 7.2$$

where vo(t) in the amplifier output and R1 is the 1 kΩ summing resistors. For a 2 Vp.p input, the buffers amplifier output of the TAD-32 is of the order of 5 Vp.p. In order to maintain the summing amplifier stability, the output voltage should not exceed the supplies rail voltage of the amplifier, and to achieve this, R2 should not exceed 100 Ω. However, the required filter functions, such as that of the sine filter coefficients range between 0 to 1 kΩ, and that requires R2 to have such a small value that the amplifier becomes unstable. Alternatively, the summing resistors used should have larger values, but this will be in conflict with the taps loading requirement, and produce cross-talk between taps, which inevitably causes the deterioration of the filter's signal to noise ratio. At this stage the use of virtual earth summing amplifier has been abandoned, and an alternative summing technique is considered. In order to solve the conflicting requirements in the tap output circuit, use is made of transistor summing amplifiers, Fig. 7.4. In order to meet the two requirements, 1 kΩ potentiometers are used for loading the taps, and to ensure low current through the potentiometers, the summing junction

node is pulled up to 6 V through transistors (T1 to T4). In this way the base current of the summing transistors (T5 to T8) are reduced. The voltage appearing on the differential amplifier inputs, are proportional to the base current of the summing transistors.

In order to obtain the required transversal filter performance, the filter input signal frequency is band limited to avoid signal distortion due to aliasing. The frequency band limiting can be achieved by the use of second order Butterworth low-pass filters having a cut-off frequency (-3 dB attenuation) of one half of the sampling frequency, i.e. 2 kHz. This filter thus adequately meets the requirement for the avoidance of errors due to signal aliasing.

7.3.2 CCD Filters hardware minimization

As described in Chapter 5, 12 FIR filters are required to realize the distance protection solution for a full three phase scheme. In order to minimize the amount of hardware used, the use of one device for two filtering functions has been considered, by weighting each of 16 taps via a chain of resistors. In this way each device performs the convolution of a relaying signal with sine and cosine reference waveforms. In this respect it must be noted that every other tap is used for each filter, i.e. taps 1, 3, ..., 31 are used for the cosine convolution filter and taps 2, 4, ..., 32 are used for the sine convolution filter. Since each device performs two filtering functions, the CCDs are clocked at 8 kHz to maintain the required 4 kHz sampling rate.

7.4 EXTRACTION FREQUENCY OPTIMIZATION

As described in Appendix 7, the extraction frequency for the finite Fourier Transform is, in theory, arbitrary. The choice of the extraction frequency is governed by the relaying term D(k), Eqn. 4.29. It is desirable that D(k) has the maximum possible magnitude, in order to maintain the performance accuracy at low level signals associated with high system impedance ratio. As shown in Appendix 7, D(t) can be expressed by Eqn. A7.18:

$$D(t) = I_p^2 \, (A^2 - B^2) \, \mathrm{SIN}(\omega_0 T_s) \qquad \text{--- } 7.3$$

where

$$A = \frac{\mathrm{SIN}(\omega_e - \omega_0)}{(\omega_e - \omega_0)} \qquad \text{--- } 7.4$$

$$B = \frac{\mathrm{SIN}(\omega_e + \omega_0)}{(\omega_e + \omega_0)} \qquad \text{--- } 7.5$$

Eqn. 7.3 shows that one of the terms which affects the magnitude of D(t) is $(A^2 - B^2)$. Fig. A7.2 shows that for a given window width T_w, this term has maximum magnitude at about $f_e = 1/2T_w$, and the choice of any other extraction frequency leads to attenuating D(t).

7.5 FILTER COEFFICIENTS ADJUSTMENT

The realization of FIR filters requires a set of tap weights in the discrete-time domain (sine and cosine reference waveforms) for the extraction of the Fourier Transform components. These are defined by Eqns. 4.5 and 4.6, which are expressed as:

$$v_1(t) = \int_0^{T_w} v(t-\tau) \, h_1(\tau) \, d\tau = \int_0^{T_w} v(t-\tau) \, \mathrm{COS}(\omega\tau) \, d\tau \qquad \text{--- } 7.6$$

$$v_2(t) = \int_0^{T_w} v(t-\tau)\, h_2(\tau)\, d\tau = \int_0^{T_w} v(t-\tau)\, \mathrm{SIN}(\omega\tau)\, d\tau \qquad \text{--- 7.7}$$

In order to produce the required filter function, it is necessary to adjust the tapping resistors to produce a weighting sequence $(h_0, \ldots, h_n)$.

The filter coefficients are adjusted by a specially designed circuit shown in Fig. 7.5. Fig. 7.6 shows the process timing diagram. The filter coefficient adjustment circuit injects a pulse of 250 μs duration at 8 ms intervals. As described in Appendix 6, Section A6.1, the CCD circuit injects a sample to the input gate at the rising edge of $\phi 1$. Thus if a pulse of $\phi 1$ duration is injected at intervals greater than the period of the filter window, no summing takes place, and the filter impulse response can be traced as the sample propagates through the device. The 8 kHz CCD clock frequency is divided into sub-frequencies and filtered via a variable cut-off frequency low-pass filter, in order to obtain the extraction frequency. Since a square wave can be represented by the summation of infinite harmonic components in the Fourier Series, the 8 kHz signal can be divided, using a binary counter to a frequency equal to the extraction, and by setting the low pass filter to a frequency equal to the extraction frequency, a synchronous sinusoidal wave can be obtained. For example, using a transformation window of 4 ms, f_e is optimally 125 Hz. By dividing the 8 kHz signal by 64, a 125 Hz square wave can be obtained, and by setting the low pass filter cut-off frequency to 125 Hz, a synchronous sine wave can be obtained. The filter coefficients are adjusted accordingly.

7.6 FIR FILTER FREQUENCY RESPONSES

In the field of filter design, it is desirable to describe the filter by plotting the frequency response.

The frequency domain properties of a linear sampled data system is conveniently obtained using the z transform. In such a system with a sampling interval T_s, the effect of delaying a sample by nT_s can be represented in the frequency domain by the transfer function z^{-1}, which can be expressed in the frequency domain by Eqn. 7.8 as:

$$z^{-1} = \text{EXP}(-jn\omega T_s) \qquad \text{--- 7.8}$$

The z-transform of a filter with coefficients h_n is then given by Eqn. 7.9:

$$H(z) = \sum_{n=0}^{N-1} h_n \, z^{-n} \qquad \text{--- 7.9}$$

which gives a frequency response given by:

$$H(j\omega) = \sum_{n=0}^{N-1} h_n \, \text{EXP}(-jn\omega T_s) \qquad \text{--- 7.10}$$

For the finite Fourier Transform process, one of the factors that affects the frequency response of the filter is the transformation window width T_w, which in turn determines the extraction frequency f_e. The filters simulated frequency response is obtained using the technique described in Sections 7.6.1 and 7.6.2.

7.6.1 Cosine filter frequency response

Consider the cosine filter impulse response $\text{COS}(n\omega_e T_s)$. The term $\text{EXP}(-jn\omega T_s)$ can be written in the form of the real and imaginary signal

components as:

$$EXP(-jn\omega_e T_s) = COS(n\omega_e T_s) - j\ SIN(n\omega_e T_s) \quad \text{---} \quad 7.11$$

Substituting Eqn. 7.11 in Eqn. 7.10 gives:

$$H_1(j\omega) = \sum_{n=0}^{N-1} COS(n\omega_e T_s)\ [COS(n\omega T_s) - j\ SIN(n\omega T_s)] \quad \text{---} \quad 7.12$$

Eqn. 7.12 has a real term and imaginary term which can be written respectively as:

$$Re\{H_1(j\omega)\} = \sum_{n=0}^{N-1} COS(n\omega_e T_s)\ COS(n\omega T_s) \quad \text{---} \quad 7.13$$

and

$$Im\{H_1(j\omega)\} = -\sum_{n=0}^{N-1} COS(n\omega_e T_s)\ SIN(n\omega T_s) \quad \text{---} \quad 7.14$$

The modulus of the frequency response $H_1(j\omega)$ can be obtained as:

$$|H_1(j\omega)| = \left[[Re\{H_1(j\omega)\}]^2 + [Im\{H_1(j\omega)\}]^2\right]^{1/2} \quad \text{---} \quad 7.15$$

and the filter phase response is given by:

$$\underline{|H_1(j\omega)} = ARCTAN\ Im\{H_1(j\omega)\}/Re\{H_1(j\omega)\} \quad \text{---} \quad 7.16$$

7.6.2 Sine filter frequency response

The frequency and phase response of the sine filter can be obtained in a similar manner, where the real and imaginary terms of the transformed components are given by Eqns. 7.17 and 7.18.

$$Re\{H_2(j\omega)\} = \sum_{n=0}^{N-1} SIN(n\omega_e T_s)\ COS(n\omega T_s) \quad \text{---} \quad 7.17$$

$$Im\{H_2(j\omega)\} = -\sum_{n=0}^{N-1} SIN(n\omega_e T_s)\ SIN(n\omega T_s) \quad \text{---} \quad 7.18$$

7.7 CCD FILTERS DYNAMIC RANGE

A distance protection relay requires a wide signal dynamic range, normally defined in terms of system impedance ratio. As shown in Appendix 4, a distance protection relay must maintain its accuracy down to 1/31 of the nominal relaying signals level. For example, a 1 Vp.p nominal relaying voltage requires an accuracy down to 30 mVp.p.

Naturally, non-ideal behaviour of CCD's causes limitations in the device performance. The CCD noise is of two sources: clock related noise which can be largely eliminated by appropriate output filtering, and random noise, which arises from the statistical noise variation. The random CCD noise can be divided into three categories [23]:

1 - Noise arising from the injection of charge into the device. As samples are introduced to the CCD, a signal distortion primarily arises at the input circuit which converts the signal voltage to a charge.

2 - Statistical variation of charge transfer from one stage to the next. When a charge packet is transferred from one stage to the next, a fraction (e) of charge is left behind and a fraction (1-e) flows into the next stage. This occurs between all adjacent stages as the charge packet proceeds along the device.

3 - Noise introduced by charge sensing circuitry, which is the most important type of random noise in tapped delay line applications, since the equivalent circuit is a capacitor discharged via a resistor. However, to overcome this problem, a buffer amplifier can be used between the CCD internal capacitor and the weighting resistor, thus minimizing charge loss during sample sensing.

The noise effects limit the CCD dynamic range. The dynamic range of a

CCD is governed by the noise level, which places a limit on the minimum sample magnitude that can be processed. Normally the dynamic range of the device is expressed as the ratio in dB of the r.m.s. noise to the r.m.s. value of the largest signal which can be processed.

In order to determine the signal processing capability of the CCD devices it is essential to measure the noise r.m.s. value. A correlation technique was used to measure the CCD noise r.m.s. value. The auto-correlation function (ACF) is defined by Eqn. 7.19 as:

$$R(\tau) = \int_0^T n(t)\, n(t-\tau)\, d\tau \qquad \text{--- } 7.19$$

The ACF at $\tau = 0$ is equal to the noise mean square value, which is equal to the variance [24], i.e.

$$\sigma^2 = \overline{X^2} \qquad \text{--- } 7.20$$

The ACF can be measured by the circuit shown in Fig. 7.7. The noise signal n(t) is split into two parts, one of which is passed through a delay network giving a time delay τ. The two parts are fed to a multiplier thus $n(t)*n(t-\tau)$ is obtained. The product is passed through an integrator with a time constant T. The output of the integral is given by Eqn. 7.21:

$$R(\tau) = \int_0^T n(t)\, n(t-\tau)\, d\tau \qquad \text{--- } 7.21$$

The above integral gives the auto-correlation function of the noise waveform. A device with a similar circuit has been used to measure the noise mean square value of the FIR filters. The input of the

filter was grounded to ensure that only the noise waveform was correlated. Fig. 7.8 shows the auto-correlation plot. The measured noise mean square value of the CCD output is 1.1 mV r.m.s., which is equivalent to -50.1 dB for 353 mV r.m.s. input. The measured FIR noise level corresponds with the signal to noise ratio as specified in the CCD data sheet (-60 dB).

7.8 SAMPLE AND HOLD CIRCUITS

Due to the nature of CCD devices, when samples are clocked through the filter stages, a clock related noise appears on the filter output. Although the clock related noise is largely removable by an appropriate filter, it has been found that if the CCD's output is sampled at the same instant, in between the clock noise spikes, using sample and hold circuits the effect of the clock noise can be largely overcome. Fig. 7.9 shows the sample and hold circuit diagram. The sample and hold circuit tracks the CCD output and holds the sample value 12 μs after the output clock strobe is initiated. The output of the sample and hold circuit is filtered by using a second order Butterworth filter, with a cut-off frequency of 2 kHz.

7.9 ANALOGUE MULTIPLEXER

Multiplexers are multiple analogue switches, which share a common output. An on chip decoder selects the appropriate channel by means of a binary code. Only one channel is activated at a time, and all channels may be activated by enable/disable control signals. The discrete process technique, for a full three phase scheme, requires analogue multiplexing of 12 finite Fourier Transform components, thus a 16-channel multiplexer has been selected (MUX-16). The multiplexer drive circuit is described

in Appendix 6, Section A6.3.

7.10 ANALOGUE-TO-DIGITAL CONVERTER A/D

The A/D converter accepts analogue input and converts it to binary format. The A/D converter is a 12-bit device, since 12-bit resolution satisfies the process accuracy required (see Appendix 4). The A/D device performs a 12-bit word conversion in 6 μs, using successive approximation technique. The A/D conversion cycles are controlled by the analogue multiplexer operation. Appendix 6, Section A6.4 describes the A/D conversion cycle initiation.

7.11 DIRECT MEMORY ACCESS (DMA) UNIT

The DMA unit consists of a bus exchange logic unit (BELU), and an address generator. The BELU provides the means by which a master gains control of the bus, using hand-shake control signals as described in Appendix 5. A DMA cycle is initiated by the A/D converter 'end of conversion' line as described in Appendix 6, Section A6.4..

The evaluation of the distance protection algorithm, requires the transfer of 12 finite Fourier Transform components to the microcomputer memory, for each processing cycle. In order to transfer these 12 components, an address generator is required. Appendix 6, Section A6.5, gives the technical descriptions of the data acquisition DMA unit.

7.12 RELAY TIMING SIGNALS

The relay timing signals are generated by the Z8002 microcomputer system timer controller, as described in Appendix 5. In order to maintain the process integrity, it is important to synchronise the performance of

the relay hardware, through a set of timing signals. Fig. 7.10 shows the relay timing diagram. In order to maintain the 4 kHz sampling rate, the CCD is clocked at 8 kHz, since each device performs two filtering functions. However, the CCD clock circuitry requires a 16 kHz clock waveform to generate the 8 kHz complementary waveforms. The filter outputs are sampled at 4 kHz, and the filter outputs are frozen 12 μs after the CCD filters output clock is initiated. The sampled filter outputs are multiplexed via a 16-channel multiplexer, scanned at 64 kHz. As an input channel is selected, a conversion command pulse is initiated 3 μs after the channel selection, to allow for the multiplexer output settling time. Following the conversion completion (6 μs), the A/D status line initiates a DMA transfer request. The relay timing also requires short duration reset signals at 4 kHz and 2 kHz, to coordinate the performance of analogue multiplexer and the data acquisition DMA unit. The microcomputer performs its dedicated task by monitoring the status of the system timer controller and coordinates the processing task.

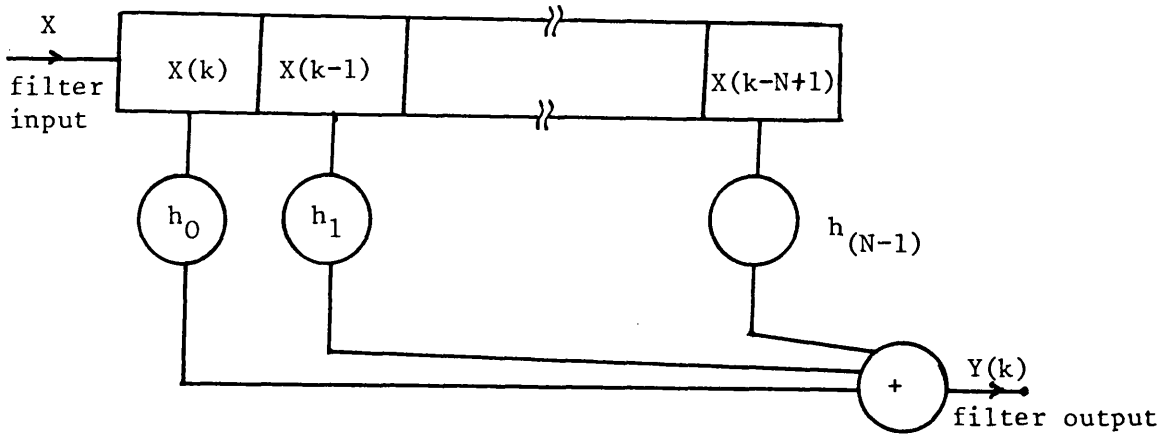


Fig. 7.1 : Functional Description of an FIR Filter

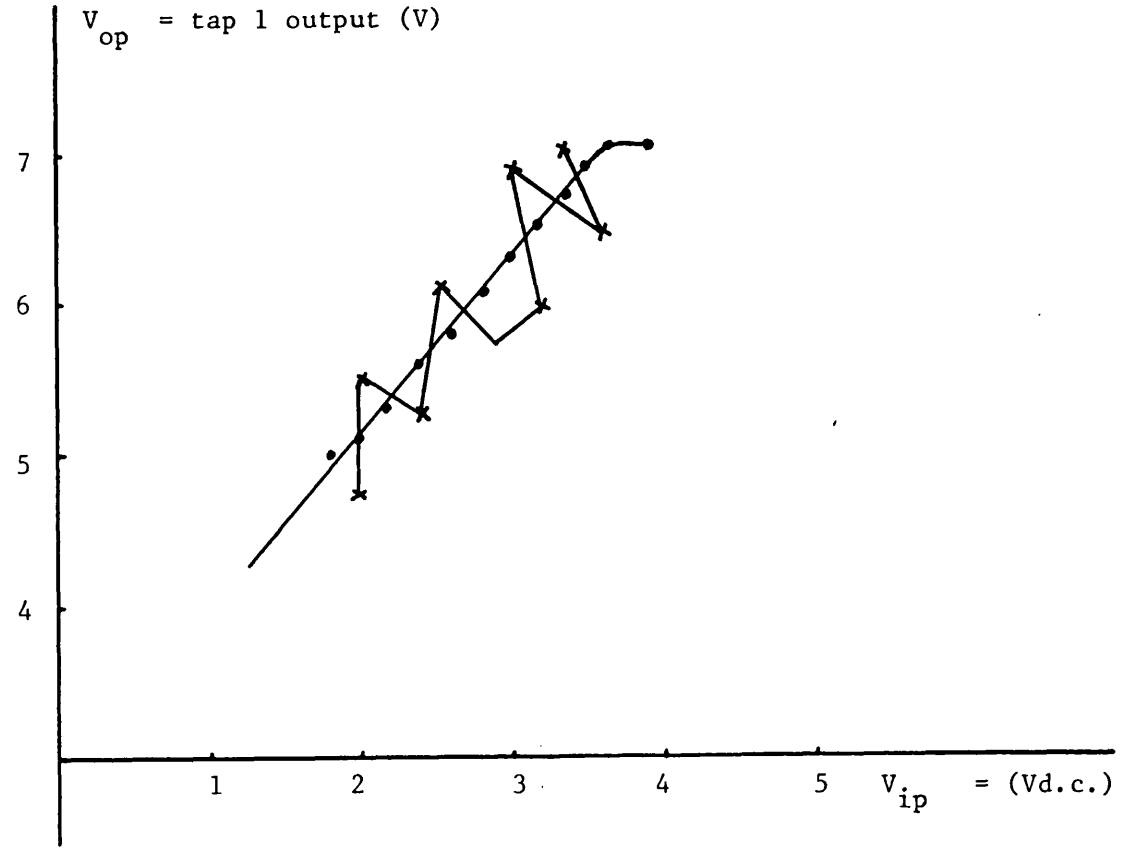


Fig. 7.2 : The effect of tap loading on taps cross-talk using d.c. input and 8 kHz sampling rate

1 kΩ

10 kΩ

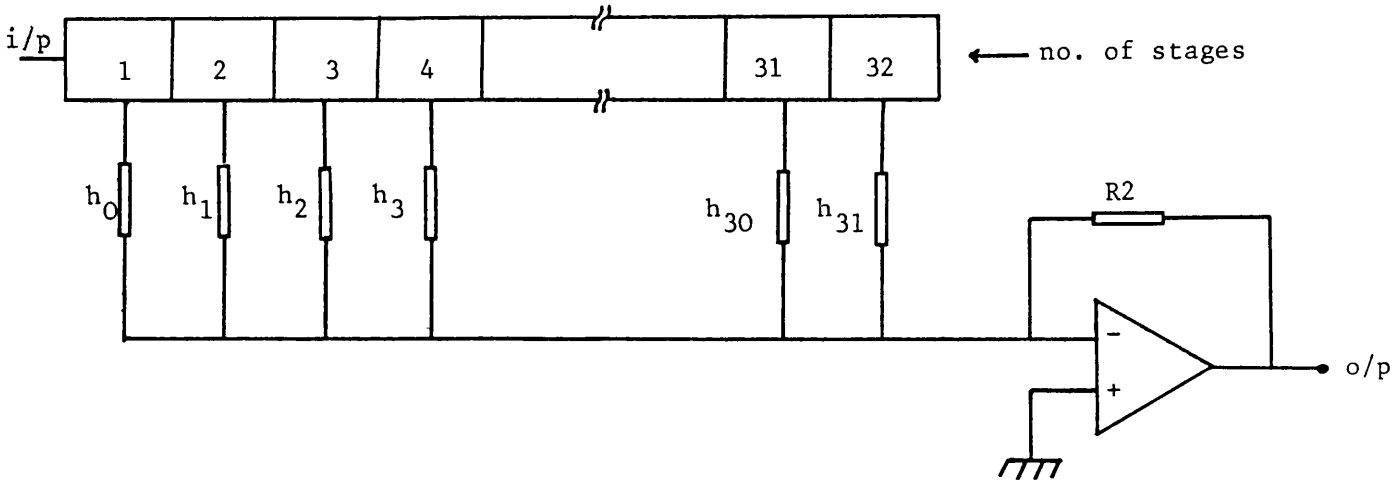


Fig. 7.3 : Virtual-earth summing amplifier

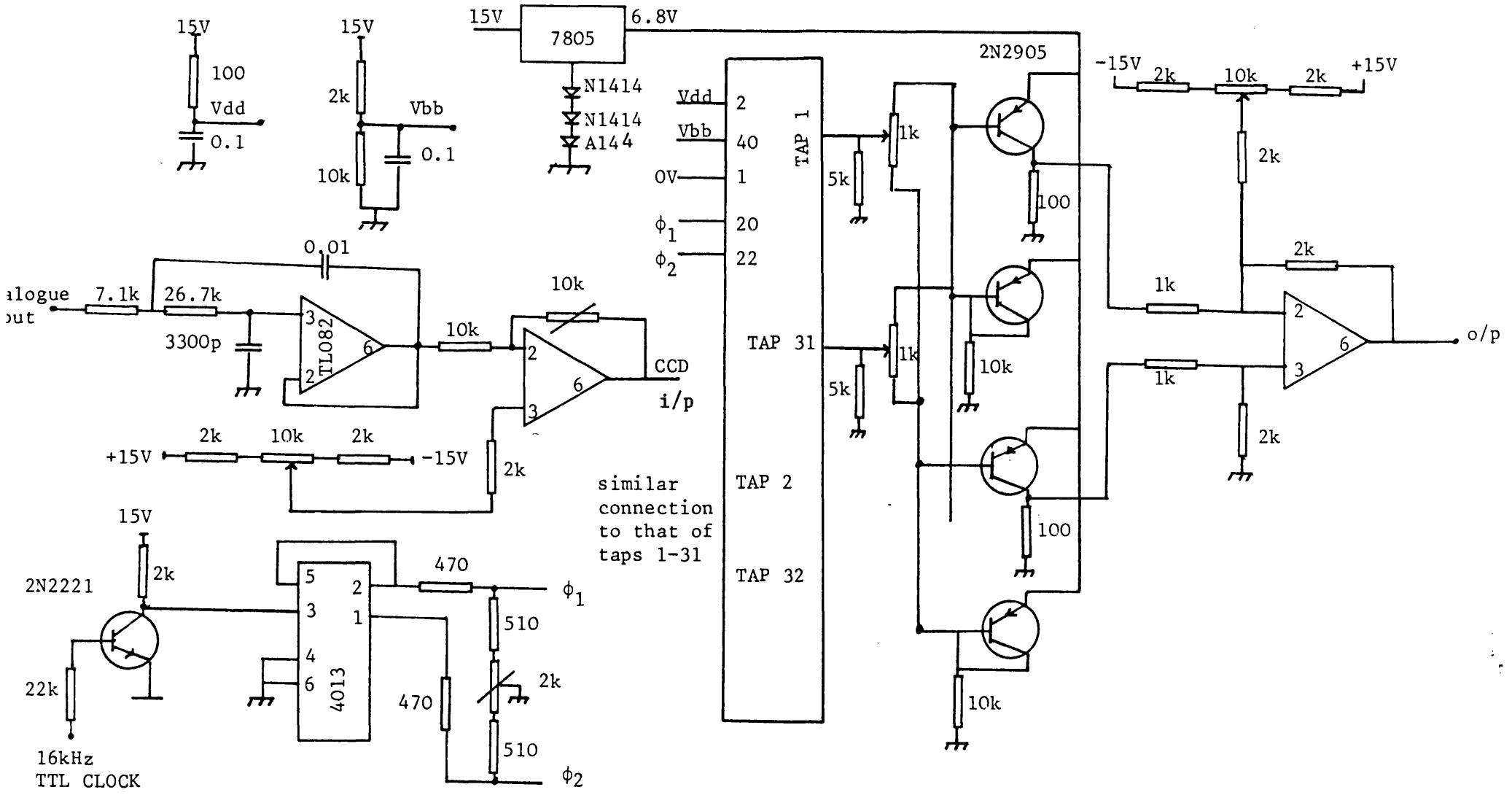


Fig. 7.4 : TAD-32 circuit diagram

All resistors are in Ω unless otherwise specified
All capacitors are in μF unless otherwise specified

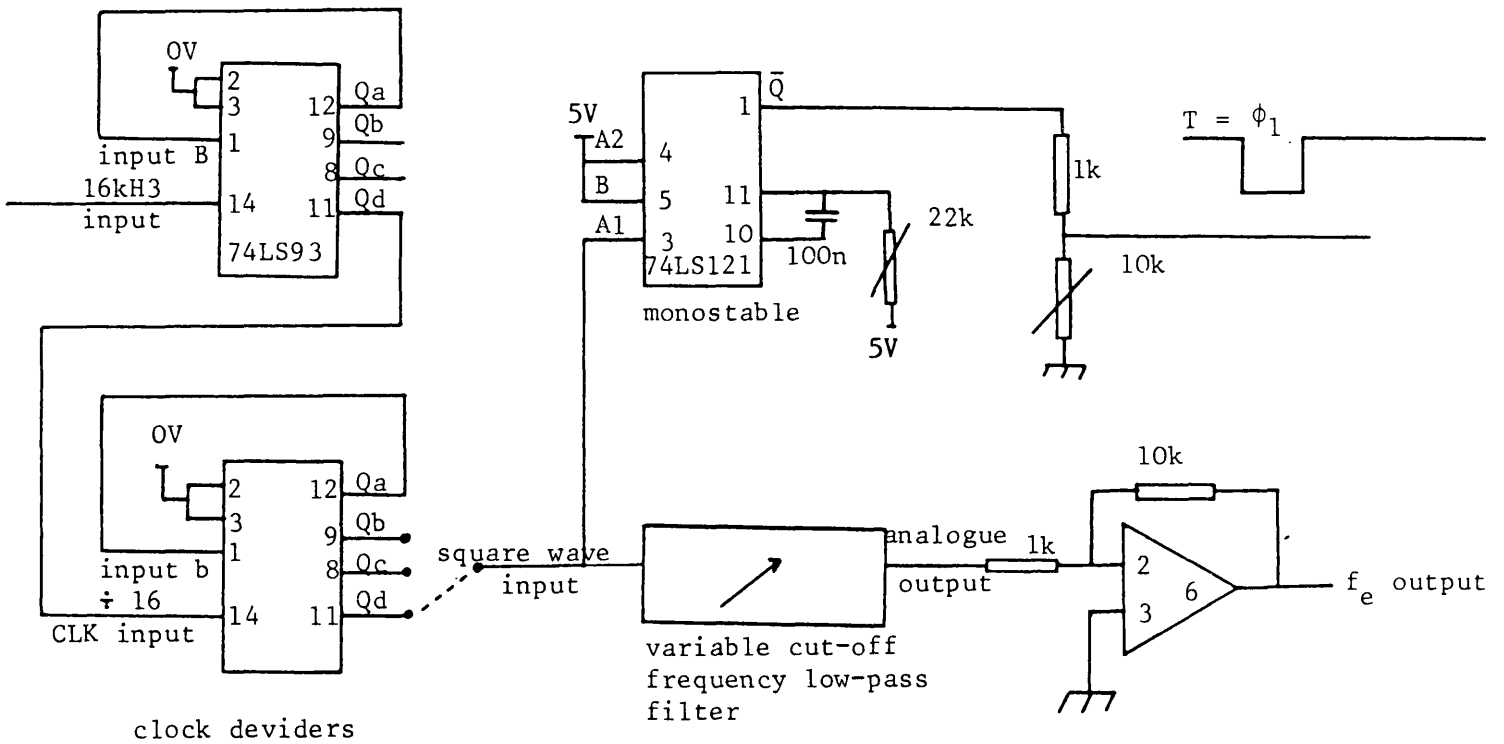


Fig. 7.5 : Filters coefficients adjustment circuit diagram

All resistors are in Ω unless otherwise specified
All capacitors are in μF unless otherwise specified

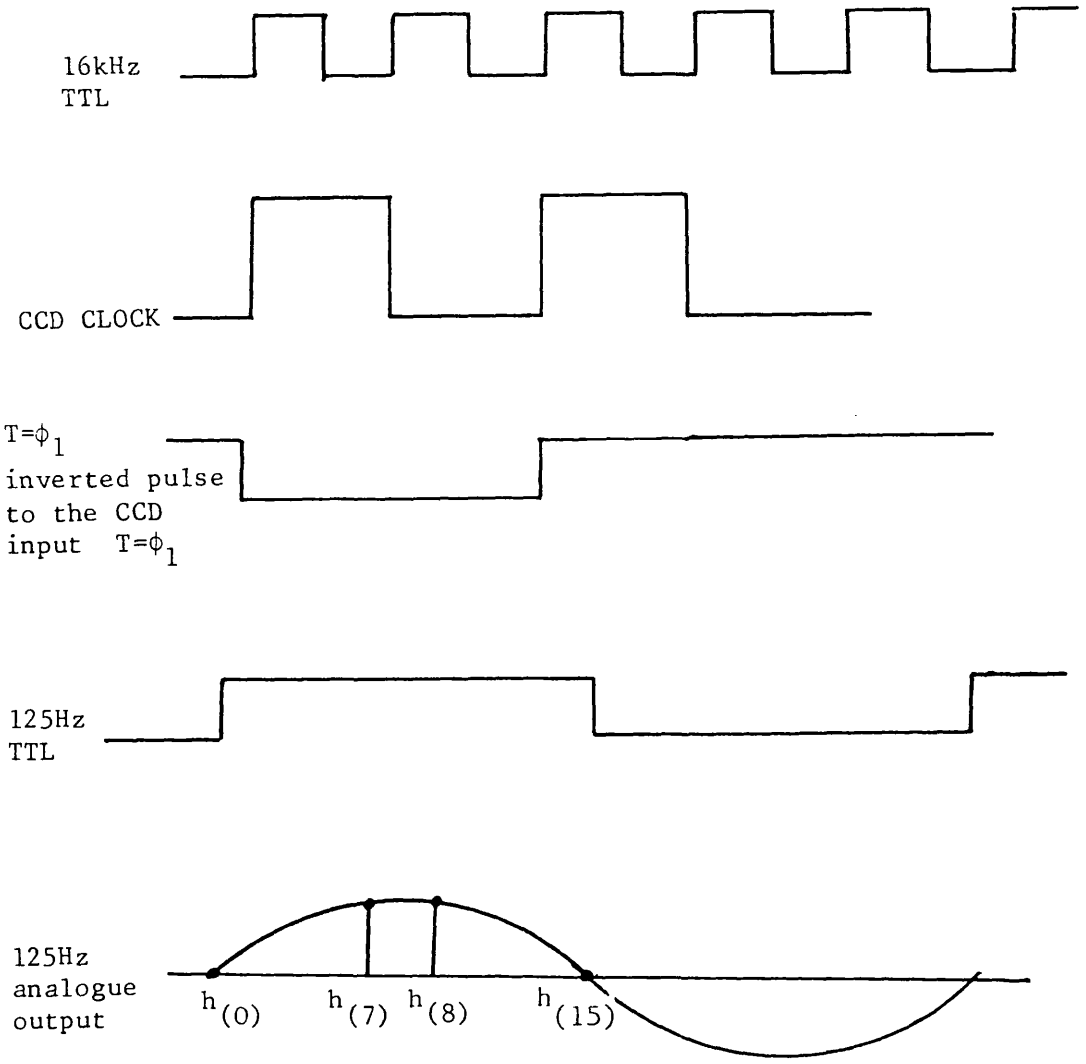


Fig. 7.6 : Filter coefficients adjustment timing diagram

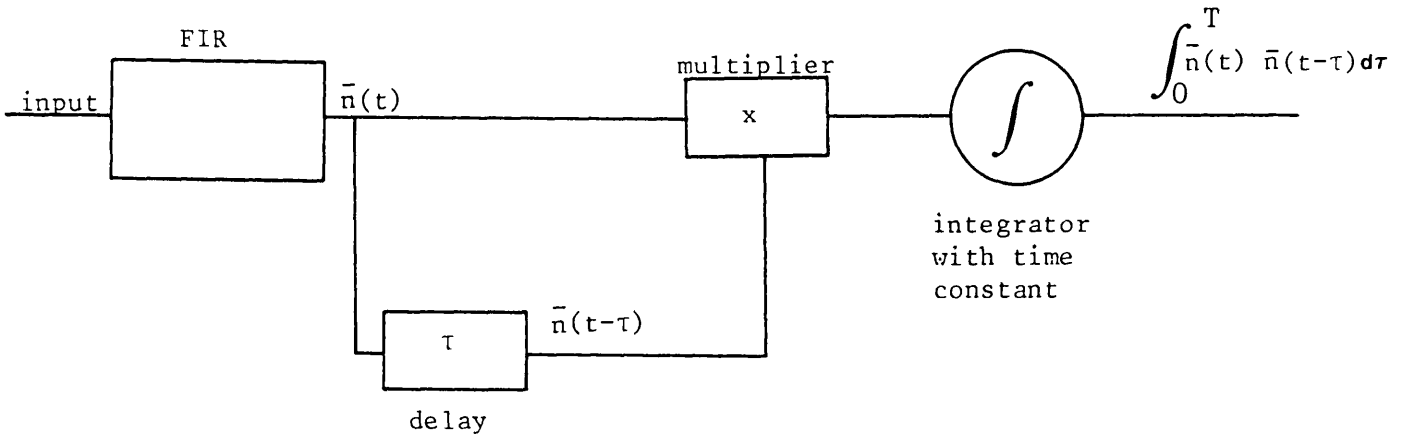


Fig. 7.7 : Auto-correlation measuring circuit block diagram

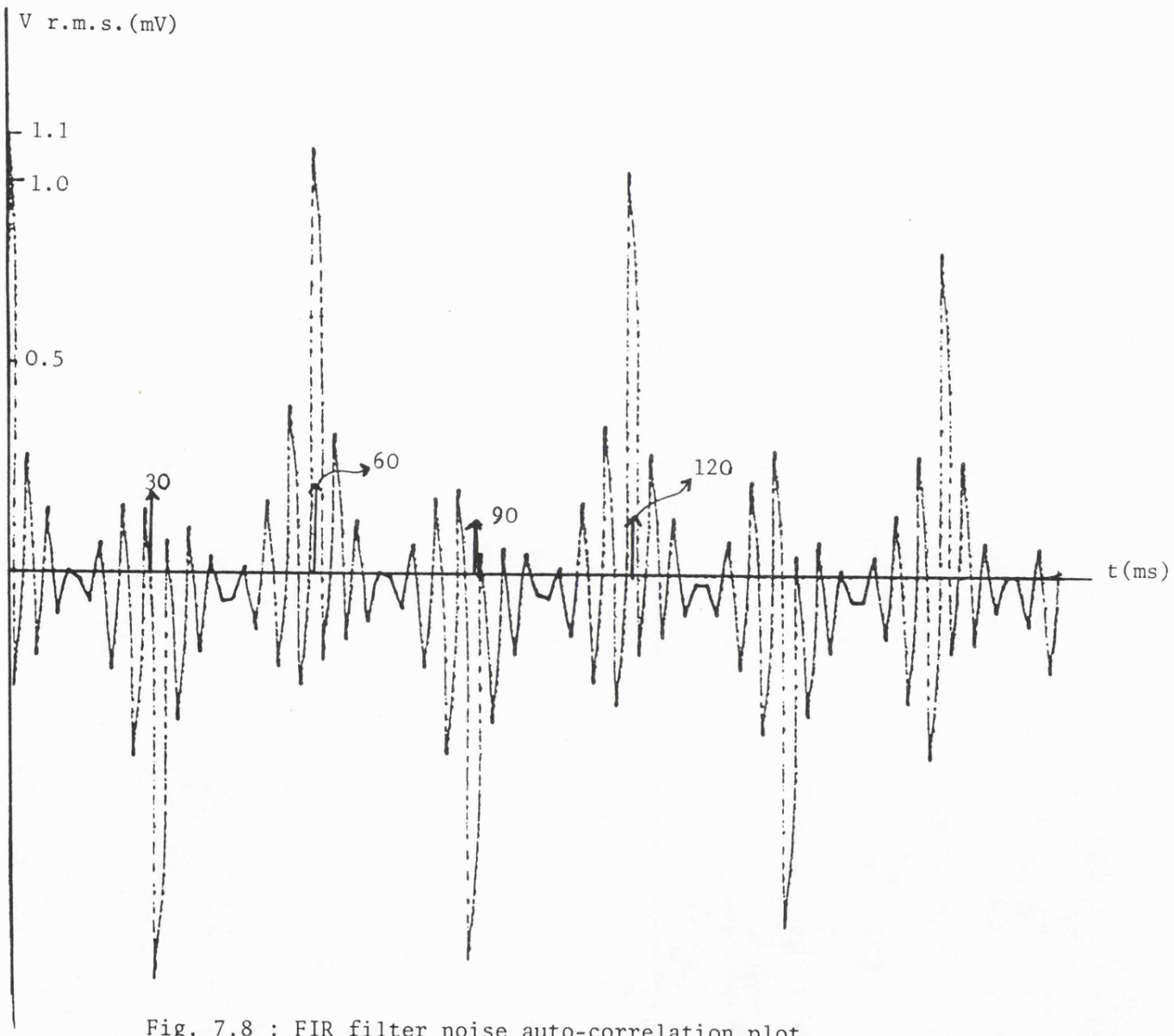


Fig. 7.8 : FIR filter noise auto-correlation plot

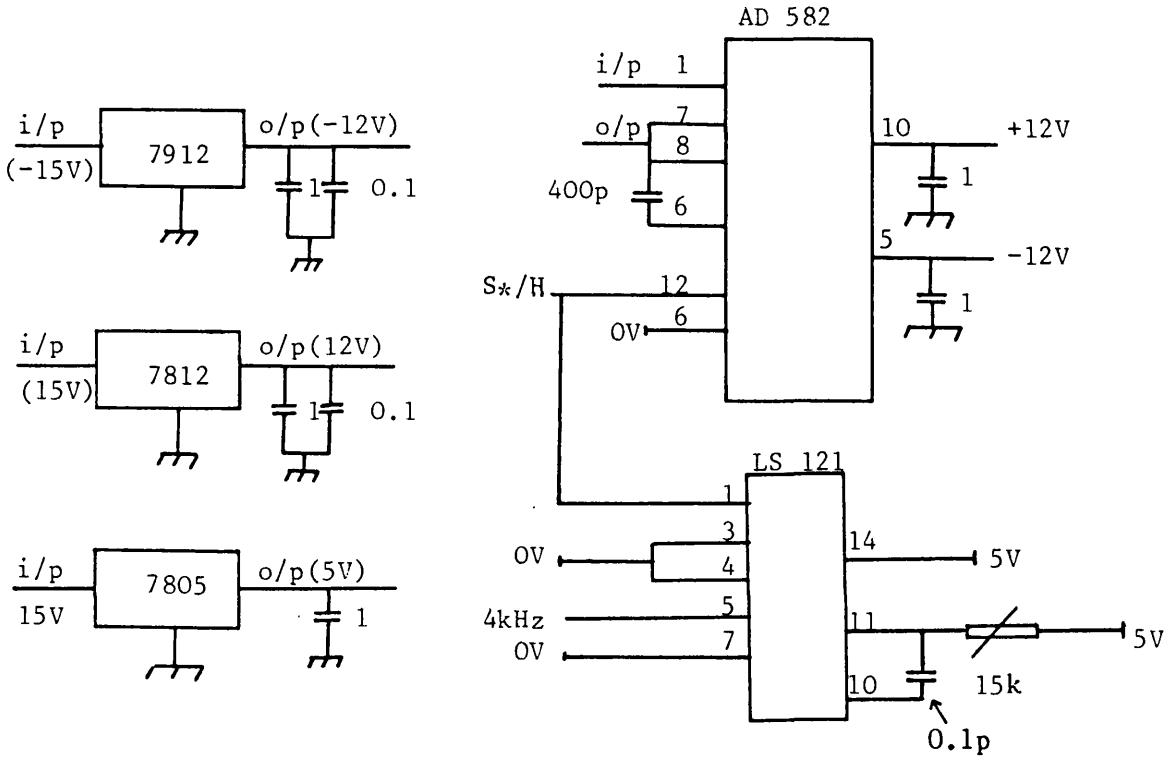


Fig. 7.9 : Sample and hold circuit diagram

All resistors are in Ω unless otherwise specified
All capacitors are in μF unless otherwise specified

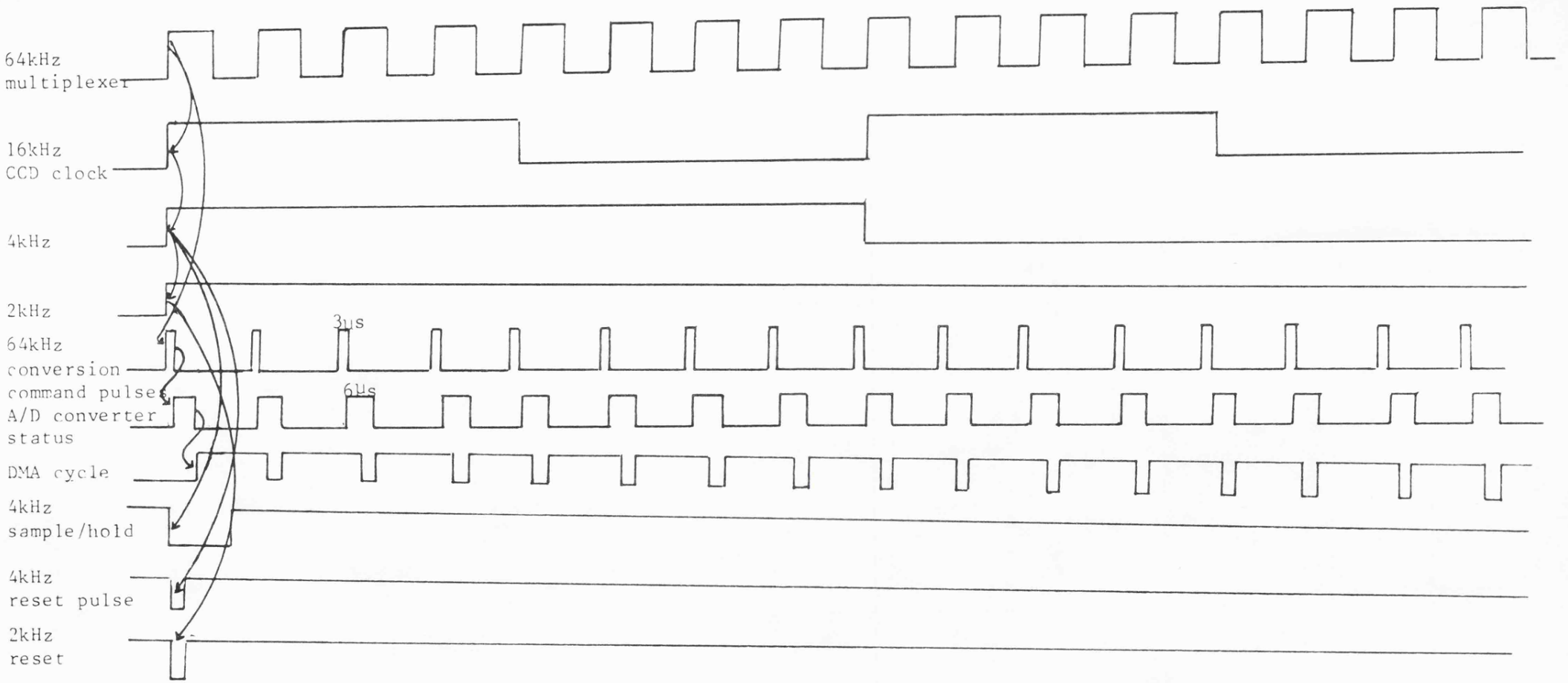


Fig. 7.10 : Relay timing signals

CHAPTER 8

RELAY TEST

8.1 INTRODUCTION

The advantage of using the finite Fourier Transform technique, for distance protection is the flexibility in the window width T_w, through which the scheme may look at the relaying signals. Previous simulation studies have been made using windows of 16, 6 and 5 samples [4, 18 and 19]. Two window widths have been selected for the evaluation of the relay performance, 16 samples window (f_e = 125 Hz) and 6 samples window (f_e = 333 Hz). The present Chapter deals with the test results of the 16 samples window, and the 6 samples window test observations are dealt with in Chapter 9. The relay performance is tested using the constraints given by Eqns. 4.34 and 4.35. The test of the constraint $LD(k)/T_s < K_4 D(k)$ in Eqn. 4.34 is performed in two parts, one for the main protection zone and one for 75% of the reactance reach to control the magnitude of the decision logic counter increment, as described in Section 4.3. For simplicity, the subscript [arc] which refers to 'a' phase residual compensated current will be omitted from the text.

8.2 PRIMARY SYSTEM SIMULATION

Fault conditions in a power system give rise to a very complicated transient phenomena in the relaying signals. For the relay test, there is a necessity for reproducing the type of waveforms which will be experienced by the protection scheme in a practical situation. For practical purposes, the relay is tested using lumped parameter and frequency domain primary system simulation [6]. The lumped parameter models give adequate facilities for normal schemes, but they do not

simulate the high frequency components and noise present immediately following a fault, to which a u.h.s. relaying scheme would be subjected. The frequency domain primary simulation gives a detailed description of the line parameter frequency variations and the high frequency phenomena subsequent to a fault occurrence. The results of this simulation technique have been verified by favourable comparison with actual fault data [6].

8.3 LINE CONFIGURATION AND FAULT TYPES

A power system configuration can vary widely in both line lengths, and source capacities. However, for the preliminary tests it was decided to investigate the relay performance in a similar manner to that of the relay simulation studies [4, 18 and 19]. For this purpose a 50 Hz, 400 kV, 128 km transmission line was chosen.

Power systems can be subjected to faults of unlimited form with variation of such parameters as fault inception angle, fault resistance and source termination. For the purpose of the relay testing, source terminations of between 5 and 35 GVA were used, in conjunction with fault inception angles of 0, 45, 90 and 135 degrees with respect to "a-phase" voltage zero were selected. For the purpose of the prototype relay testing, a single phase to earth fault only was applied.

8.4 FAULT DATA SCALING

Phase voltages and currents are provided to a conventional distance protection relay via capacitor voltage transformers (CVT's) and current transformers (CT's). The voltage interface unit reduces the input voltage signal from nominally 63.5 V r.m.s. phase to earth, to 20 V p.p

signals as required by the relay measuring circuits. The current interface may consist of a transactor and an integrator to produce an output voltage proportional to the input current. Fig. 8.1 shows the relay input interface.

For the prototype relay, the simulated fault data for a 400 kV line is fed to the relay via a Programmable Transmission Line (PTL). Once the primary system voltage and current are generated in real number format, using a main frame computer, the PTL transform the fault data to a binary format. Thus the primary voltage and current signals are constructed, via the PTL A/D converters. Moreover, the PTL allows the scaling of the voltage and current to the level required by the relay.

As shown in Appendix 8, the voltage scaling factor is 1/39191.836 and the current scaling factor is 1/1332.2. In this respect it must be noted that it is desirable that the voltage signal level is equal to that of the current for faults at the relay reach, in order to achieve the best obtainable accuracy. In order to include the effect of the CVT transients, the relaying voltage signals are processed through a CVT simulation program using parameters derived from actual CVT frequency response data. The CT simulation has not been undertaken, since the CT frequency response is of relatively wide band compared with that of the anti-aliasing pre-filter, which is set to have a cut-off frequency of 2 kHz.

8.5 RELAY SAMPLING RATE

The relay conventional hardware structure timing test showed a speed limitation. In consequence, the sampling rate had to be reduced from

4 kHz to 2.7 kHz. The reduction in the sampling rate is due to the loading of the multibus by peripherals. As shown in Fig. 5.5, the Z8002 processor, the data acquisition unit and the multiplier DMA share the same multibus and the overheads of bus acquisition by the three bus masters slows the overall relay processing speed.

8.6 16 SAMPLE TRANSFORMATION WINDOW

For the 6 ms transformation window, it is necessary to determine the filter characteristics such as the impulse response, the frequency response and the phase response, so that an in depth look into the relay performance can be obtained.

8.6.1 Filter impulse responses

The filter impulse responses $h_{1(n)}$ and $h_{2(n)}$, Figs. 8.2a and 8.2b, are obtained by evaluating Eqns. 8.1 and 8.2, which are given by:

$$h_{1(n)} = COS(n\omega_e T_s) \quad \text{--- 8.1}$$

$$h_{2(n)} = SIN(n\omega_e T_s) \quad \text{--- 8.2}$$

where n is an integer in the range 0 to 15 and the extraction angular frequency (ω_e) is 521.5 rad/sec. The CCD filter impulse responses shown in Fig. 8.2c is obtained using the technique described in Section 7.5. The noise appearing on the impulse responses Fig. 8.2c is due to a small variation in the odd-even tap output of the CCD (see Appendix 6, Section A6.2), and in the actual application, this small variation is counteracted by using the sample and hold circuits for each filter output.

8.6.2 Filter frequency responses

The filter simulated frequency responses Fig. 8.3a are obtained using the techniques described in Section 7.6. As shown in Fig. 8.3a, the two filters have different gains at the power frequency (50 Hz), which is attenuated by 5 dB through the cosine filter and attenuated by 0.7 dB through the sine filter. However, if both voltage and current transform components are attenuated similarly by the sine and cosine convolution filters, the process would not be in error, as described in Appendix 8. The measured frequency responses of Fig. 8.3b show similar patterns compared with the simulated frequency responses. The small differences between the simulated and the measured responses are due to the measurement errors such as in adjusting the sampling clock rate, the frequency generator accuracy and the effect of using a low pass filter for the CCD output circuit.

As shown in Appendix 3, exponential offset component in the relaying current signals, can cause the term D(k) to approach zero or obtain a negative magnitude, which in turn causes errors in the constraints involving D(k). With reference to Fig. 8.3a, it can be seen that the cosine filter has a -20 dB attenuation at 0 Hz, whereas the sine filter shows no attenuation at this frequency. In order to remedy the effect of the exponential offset and to ensure that D(k) remains unipolar, the high pass of Fig. 8.4 filter was used with a cut-off frequency of 4 Hz. The use of high pass filters accentuates high frequency noise which consequently increases the differencing noise involved in the estimation of D(k). In order to minimize this error, the high pass filter output is cascaded with low pass filters having a 1 kHz cut-off frequency in series with first order R-C filter with a cut-off frequency

of 750 Hz as shown in Fig. 8.4. In order to ensure that only positive D(k) is processed, a D(k) threshold of positive 2 digital conversion levels is set, since negative D(k) causes the decision logic counter to be decremented immediately.

8.6.3 Filter phase responses

The filter phase response Fig. 8.5 is obtained using the technique described in Section 7.6. The phase characteristics of a filter are specified in terms of the phase shift $T_d(\omega)$ at frequency ω defined as:

$$T_d(\omega) = \frac{d\phi}{d\omega} \qquad \text{--- 8.3}$$

From Fig. 8.5 we have 27 and -50.4 degrees phase shift associated with the cosine and sine filters, at 50 Hz, respectively. Thus the overall phase shift of the two filters ($\phi_{11} - \phi_{12}$) is 77.4 degrees.

8.7 LUMPED PARAMETER MODEL TEST

The lumped parameter simulation, Appendix 9, is performed using a single end fed 128 km, 400 kV line, having a self impedance of $Z_{s\ell} = 49.46$ ohm, corresponding to 80% of the line length (see Appendix 1).

Initial tests showed that random increments in the decision logic counter occurred during the pre-fault period and the counter could reach the tripping level of 5 counts. This random increment was due to noise in the relay hardware. Consider the constraint of Eqn. 8.4,

$$LD(k)/T_s < K_4\, D(k) \qquad \text{--- 8.4}$$

The test of this constraint involves the use of D(k) which requires the current signals $i_1(k)$, $i_2(k)$, $i_1(k\text{-}1)$ and $i_2(k\text{-}1)$. The pre-fault

current samples are very small in magnitude, compared with the post-fault current samples. This in turn causes the logical comparison for this constraint to be dictated by the instantaneous noise levels in the current samples. In order to overcome this problem, a threshold of 8 conversion levels has been set for D(k). The D(k) threshold was adequate to prevent pre-fault counter increments, but it influences the relay operation at high SIR.

8.7.1 Case 1 : Relay operating time against fault location at specific fault inception angles using 5 GVA source capacity

Fig. 8.6 shows the relay operating time for fault inception angles of 0, 45, 90 and 135 degrees. The fault locations are close-up faults (0% of the relay reach), 35%, 50%, 75% and 100% of the relay reach. The fastest relay operating time is for a close-up fault (approximately 7 ms). The relay operating time increases as the distance to the fault increases, particularly for faults between 75% and 100% of the relay reach, the outer region of the impedance plane, where the counter is incremented in steps of one.

8.7.2 Case 2 : Relay operating time against fault location at specified fault inception angles for 35 GVA source capacity

Fig. 8.7 shows the relay operating time for 0, 45, 90 and 135 degree inception angles. The fault location are 0%, 35%, 50%, 75% and 100% of the relay reach. The fastest operating time is achieved for close-up faults. Similar operating time characteristics to Case 1 (Section 8.7.1) have been observed.

8.8 DOUBLE END FED, 3 PHASE SYSTEM EVALUATION

The double end fed, 3 phase system tests were carried out using a 128 km, 400 kV line fed from 5 and 35 GVA source capacities as shown in Fig. 8.8. The positive phase sequence impedance at the relay reach is 29.3 Ω. The fault locations tested were 0%, 35%, 50%, 75% and 100% of the relay reach, for 0, 45, 90 and 135 degrees inception angles.

8.8.1 Case 1 : 5 GVA Source capacity at the relaying point and 35 GVA at the remote end of the line

Fig. 8.9 shows the relay response for these types of fault. The use of a relatively low source capacity (5 GVA) represents a very onerous case from the relaying point of view, because the system voltage is severely distorted due to the travelling wave components. However, the observed relay operation shows a similarity to that derived from 5 GVA lumped parameter model (see Section 8.7.1). The similarity in relay operating time is due to the fact that the 6 ms filters have the first zero in the frequency response occurring at 200 Hz, which provides a drastic attenuation for the noise arising from the fault induced travelling wave.

8.8.2 Case 2 : 35 GVA Source capacity at the relaying point and 5 GVA at the remote end of the line

Fig. 8.10 shows the relay operating time for 35 GVA source capacity at the relaying point. The relay operating time is similar to that derived using the lumped parameter model (see Section 8.7.2), for similar reasons to those of Section 8.8.1.

8.9 ALGORITHM RESPONSE TO CURRENT CLIPPING

As shown in Appendix 9, the post-fault current for the lumped parameter model is given by the following equations:

$$i(t) = I_p \left[\text{SIN}(\omega_0 t+\theta-\phi) - \text{SIN}(\theta-\phi)\ \text{EXP}(-t/\tau)\right] \quad \text{---} \quad 8.5$$

where

$$\phi = \text{ARCTAN}\ (X/R) \quad \text{---} \quad 8.6$$

$$\tau = L/R \quad \text{---} \quad 8.7$$

and

$$I_p = V_p/(Z_{s\ell}+Z_s) \quad \text{---} \quad 8.8$$

Eqn. 8.5 shows that the post fault current magnitude is a function of the maximum current which is determined by the line voltage, source capacity at the relaying point and the distance to fault. As described in Appendix 8, it is desirable that for a fault at the relay reach, the current signal level is equal to that of the phase voltage signal. The output from the interface circuits are limited by the operation amplifier supply voltage, (20 Vp.p). Thus for close-up, high source capacity faults at the relaying end, clipping is inevitable in the current signals.

It can be seen from Eqn. 4.15, D(t) is formulated as:

$$D(t) = i_1(t)\ i_2'(t) - i_1'(t)\ i_2(t) \quad \text{---} \quad 8.9$$

As the current signal clips, the rates of change in the current signals $i_1'(t)$ and $i_2'(t)$ becomes very small and approach zero if the clipping

persists, as shown in Fig. 8.11. When a fault occurs, D(k) converges to the post-fault value but as the current signal clips, the magnitude of D(k) reduces such that the fault appears to be out of zone. Fig. 8.12 shows that when the clipping affects both the sine and cosine filter outputs, the decision logic counter starts decrementing indicating an out of zone fault. Nevertheless, for u.h.s. operation, for 128 km line close-up faults, the decision logic counter reaches a trip level before clipping persists. However, for longer lines, fast operations for close-up faults is in doubt.

8.10 RELAY RESPONSE TO RESISTIVE FAULTS

In practice, power system faults are associated with an additional resistive component and a distance protection relay must cater for these types of resistive faults.

The fault resistance tests were performed using a double end fed, 128 km, 400 kV line, for 0 and 90 degree inception angles, since it has been found that the relay operating times do not vary considerably from those for 45 and 135 degree inception angles and 0 and 90 degree inceptions represent two extreme cases with respect to the relaying current exponential offset and the travelling wave components respectively. The relay operating time is obtained for 0%, 25%, 50%, 75% and 100% of the relay reach and for 10, 20, 30 and 40 Ω resistive faults. For some types of resistive fault, the relay operating time is consistent and for others, two operating times are given to show the minimum and maximum operating time.

8.10.1 Case 1 : 35 GVA Source capacity at the relaying point and 5 GVA at the remote end of the line

Figs. 8.13a and 8.13b show the relay operating time for 0 and 90 degree inception angles respectively. The relay operates for 40 Ω resistive faults for up to 25% of the relay reach, for the 90 degree inception angle and operates for 40 Ω resistive faults for up to 50% of the relay reach for the 0 degree inception angle. The relay operates for faults of up to 30 Ω resistance, for up to 75% of the relay reach, but for 100% of the relay reach, the relay operates for resistive faults of up to 20 Ω only.

8.10.2 Case 2 : 5 GVA Source capacity at the relaying point and 35 GVA at the remote end of the line

Figs. 8.13c and 8.13d show the relay operating time for 0 and 90 degree inception angles respectively. For close-up faults, the relay operates for up to 40 Ω resistive fault. The relay operates for up to 30 Ω for voltage minimum faults at 25% of the relay reach, but not for voltage maximum faults. However, the resistive coverage of the relay reduces as the fault distance increases and for a 100% of the relay reach the relay does not operate for 10 Ω fault resistance.

8.10.3 Relay resistance fault coverage assessment

As shown in Appendix 10, the impedance seen by the relay ($Z\ell_1$ meas.) in the event of resistive fault is given by:

$$(Z\ell_1 \text{ meas.}) = \alpha(Z\ell_1) + R_f + (I_2/I_1)\, R_f \qquad \text{--- } 8.10$$

where α is the fault distance from the relaying point, $Z\ell_1$ and R_f are the positive phase sequence impedance and the fault resistance respec-

tively, I1 and I2 are the local and remote end feeder fault currents respectively. As can be seen from Eqn. 8.10, for a solid fault ($R_f = 0$) the impedance seen by the relay is proportional to the positive line sequence impedance. However, most faults involve some fault resistance and the relay measures an additional component, one of which is proportional to the source fault current ratio $|I2/I1|$, as given by Eqn. 8.10. In practice, power system faults involve a fault resistance, characterized by the arc resistance, which has a value given by the Warrington formula [26] as:

$$R_f = 287 \frac{\ell_0}{i(arc)^{1.4}} \qquad \text{--- 8.11}$$

where ℓ_0 is the arc length in centimeters (280.4 cm arc horn for 400 kV lines), and i(arc) is the arc current. For e.h.v. applications, faults often involve strong arc currents. Hence relatively low fault resistances are involved [27], and the relay operating time will be similar to that for solid faults. However, it is difficult for distance protection relays to provide a satisfactory protection against abnormal resistive faults, such as those involving vegetation or long arcs caused by bush fires, where very high resistance can be involved.

8.11 RELAY DIRECTIONAL STABILITY

A distance protection relay must maintain consistency of performance for faults within the protected zone. However, the constraints of Eqns. 4.34 and 4.35 cause unwanted operation for reverse faults (faults behind the relay). In order to make the relay truly directional, the principle of directional reactance $X_m(k)$ must be implemented. The directional reactance measurement uses the delayed samples of the transformed voltage in conjunction with undelayed samples of the transformed current

components. The directional reactance technique can be implemented by using a voltage memory bank (VMB), to hold the pre-fault samples of the transformed components. The directional reactance Xm is compared with the directional reactance value X_0, and an additional constraint is added to that of Eqns. 4.34 and 4.35 in the following form:

$$X_m(k) > X_0 \quad \text{--- 8.12}$$

where X_0 = 1.5 Ω [4]. Eqn. 8.12 can be written as follows:

$$\omega_0 L (k) > X_0 \quad \text{--- 8.13}$$

Multiplying Eqn. 8.13 by D(k) and dividing by $\omega_0 T_s$ gives:

$$L_m(k)D(k)/T_s > Km\ D(k) \quad \text{--- 8.14}$$

where $Km = X_0/\omega_0 T_s$. From Eqn. 4.30, the term $L_m(k)D(k)/T_s$ can be written as:

$$L_m(k)D(k)/T_s = v_2(k-N)\ i_1(k) - v_1(k-N)\ i_2(k) \quad \text{--- 8.15}$$

where v(k) is the current voltage sample, and v(k-N) is the Nth previous sample. For the prototype relay, samples for one prefault voltage power cycle are used and for a 2.7 kHz sampling rate 54 samples correspond to one power frequency cycle. Eqn. 8.15 can be written as:

$$L_m(k)D(k)/T_s = v_2(k-54)\ i_1(k) - v_1(k-54)\ i_2(k) \quad \text{--- 8.16}$$

The directional integrity of the relay can be maintained by using the directional reactance, since, for forward faults, the directional reactance lies in the first two quadrants of the impedance plane. Conversely, for reverse faults, the directional reactance lies within

the third and fourth quadrants of the impedance plane [4]. Thus, the behaviour of the directional reactance provides a discriminative technique for forward or reverse fault detection.

8.11.1 Voltage memory bank implementation

The estimate of the directional reactance, Eqn. 8.16 requires the samples for one pre-fault power frequency cycle of the phase voltage or 54 samples at a 2.7 kHz sampling rate. The VMB is a 108 word long ring buffer, holding the samples for one power frequency cycle of the Fourier Transform components $v_1(k-54)$ and $v_2(k-54)$. In this respect, it must be noted that due to signal symmetry, $v_1(k)$ and $v_2(k)$ can be dumped in the same buffer location of the VMB where $v_1(k-54)$ and $v_2(k-54)$ are retrieved.

8.11.2 Reverse fault stability

The relay reverse fault stability and the directional reactance behaviour has been tested for close-up faults, since this type of fault is onerous from the point of view that the phase voltage suffer from a complete collapse, during which the behaviour of the directional reactance is unpredictable when the VMB runs out the pre-fault voltage samples.

8.11.3 Directional reactance behaviour for reverse faults

Figs. 8.14a to 8.14d shows the behaviour of the term $L_m(k)D(k)/T_s$ for 5 and 35 GVA source capacities, at 0 and 90 degree inception angles. It can be clearly seen that this term converges to a negative magnitude, following fault inception. Thus the constraint of Eqn. 8.12 will not be satisfied. Figs. 8.15a and 8.15b show the behaviour of the decision logic counter for a 5 GVA source capacity, at 0 and 90 degree inception

angles. For Vmin. faults the constraints of Eqns. 4.34 and 4.35 are satisfied and the decision logic counter reaches the trip level at approximately 6.9 ms, while the constraint of Eqn. 8.12 inhibits the counter increment for approximately 35.6 ms. For 90 degree inception angle, the relay reaches a trip level at 8.45 ms, but the constraint of Eqn. 8.12 inhibits counting for 32 ms. For a 35 GVA source capacity, Figs. 8.15c and 8.15d, the relay reaches the trip level at 6.1 ms and 8.45 ms for 0 and 90 degree inception angles respectively, but the constraint of Eqn. 8.12 inhibits counting for approximately 30 ms. As shown in Figs. 8.15a to 8.15d, the decision logic counter response to the fault after the VMB runs out of voltage samples. The relay response to a close-up reverse fault are due to the complete collapse in the phase voltage and the low harmonics of the CVT transient. For the actual technique application, more than one pre-fault cycle VMB is required, as necessitated by operational requirements.

8.11.4 Forward fault directional response

For forward faults, the directional reactance $X_m(k)$ lies in the first two quadrants of the impedance plane. However, the directional constraints can impose a speed restriction on the relay performance. For 5 and 35 GVA source capacities and 90 degree inception angles, the directional constraint converges to the post fault value in approximately 3 ms for close-up faults, and the speed of the relay is not affected. For a 5 GVA source capacity and 0 degree inception angle, the directional reactance constraint converges to the post-fault value 5 ms after the fault inception for close-up faults and the relay speed is not affected. However, for a 35 GVA source capacity, the relay operating time for close-up faults, 0 degree inception angle, is

approximately 20 ms. A similar operating time is observed for a fault at 35% of the relay reach, but for a fault at 50% of the relay reach the operating time is not affected. The effect of the directional reactance constraint on the relay speed for this fault condition can be clearly seen in Fig. 8.16, where the directional reactance attains a negative magnitude 2.5 ms after the fault inception, and indicates a reverse fault for approximately 10.5 ms. When the directional reactance attains a positive magnitude after 10 ms to indicate a forward fault, it coincides with the severe clipping region of the relaying current signal, which in turn causes an error in the decision logic process as described in Section 8.9.

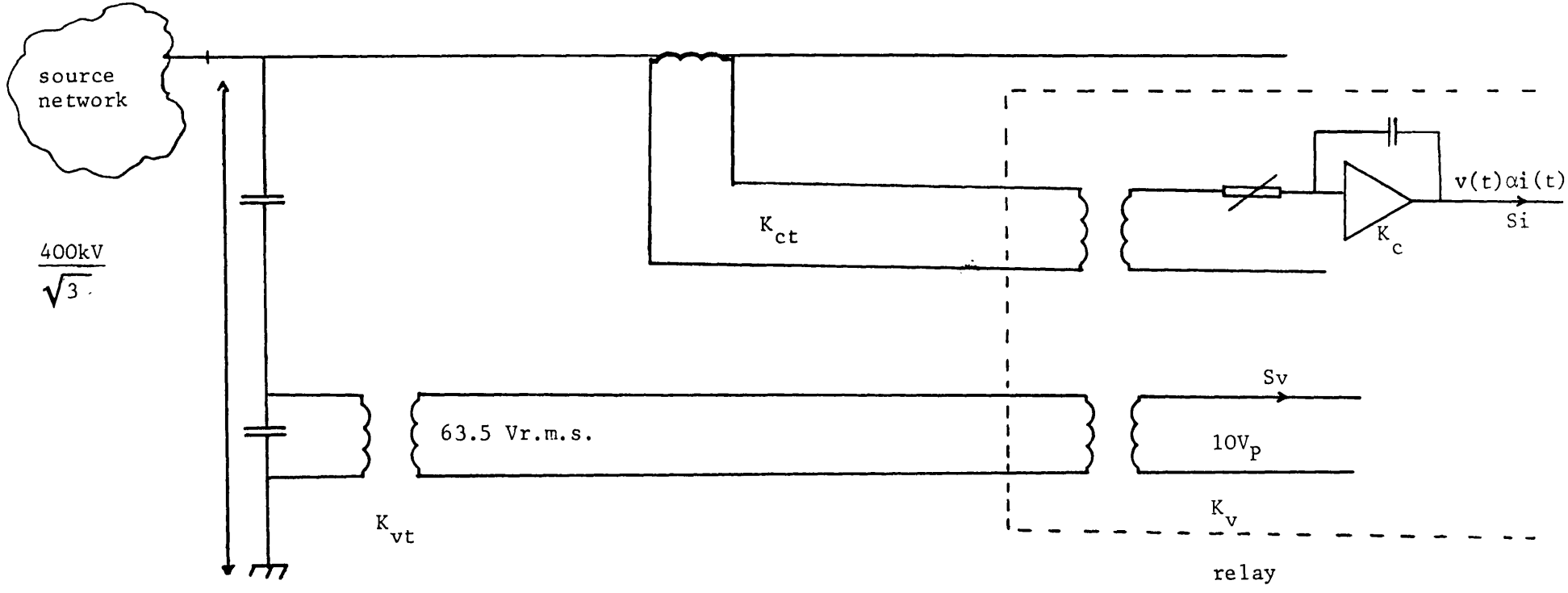


Fig. 8.1 : Relaying signals interface

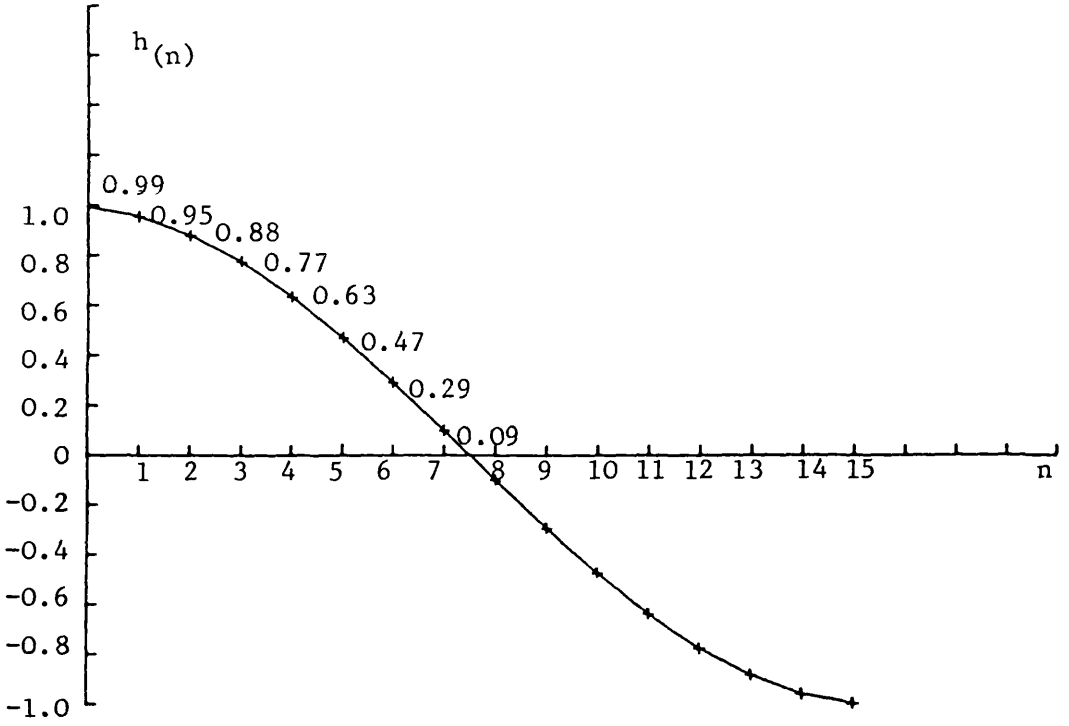


Fig. 8.2a : Cosine convolution filter impulse response
6 ms transformation window at 2.7 kHz sampling rate

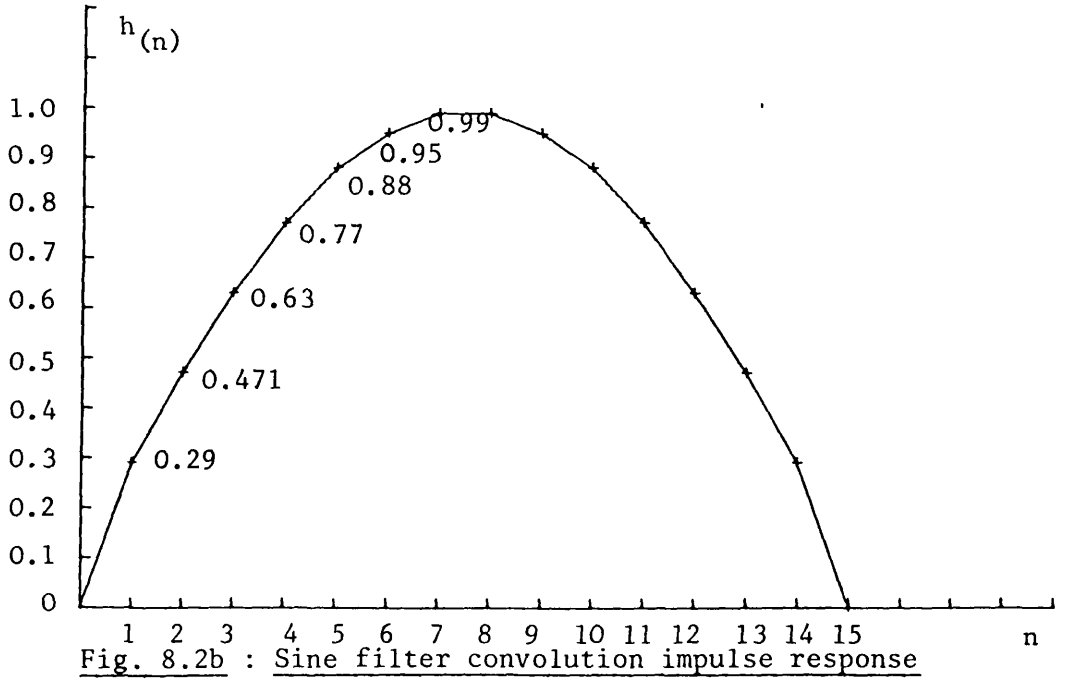


Fig. 8.2b : Sine filter convolution impulse response

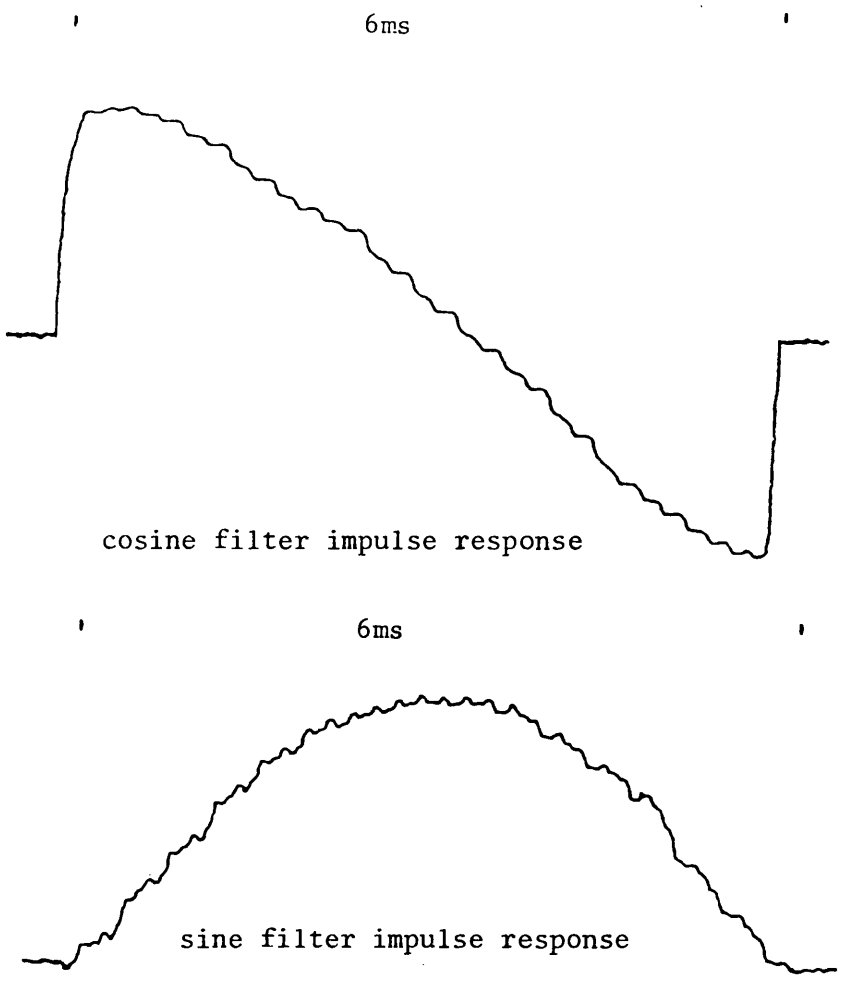


Fig. 8.2c : CCD Filter impulse responses

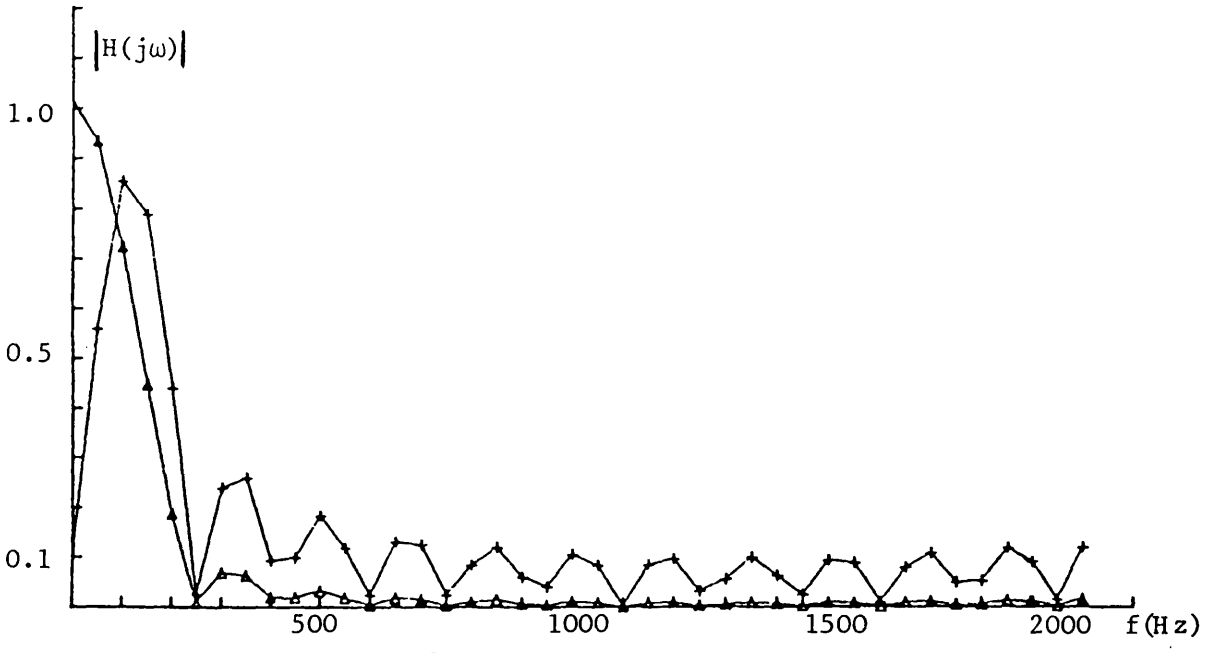


Fig. 8.3a : 6 ms transformation window frequence responses

cosine transformation filter

sine transformation filter

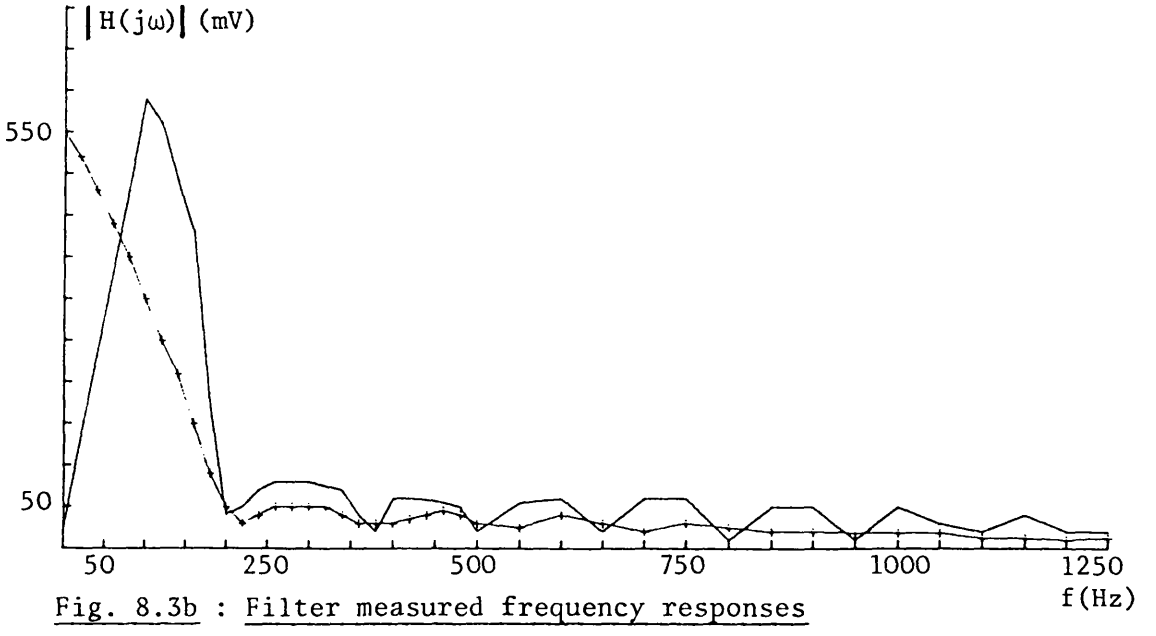


Fig. 8.3b : Filter measured frequency responses

cosine transformation filter

sine transformation filter

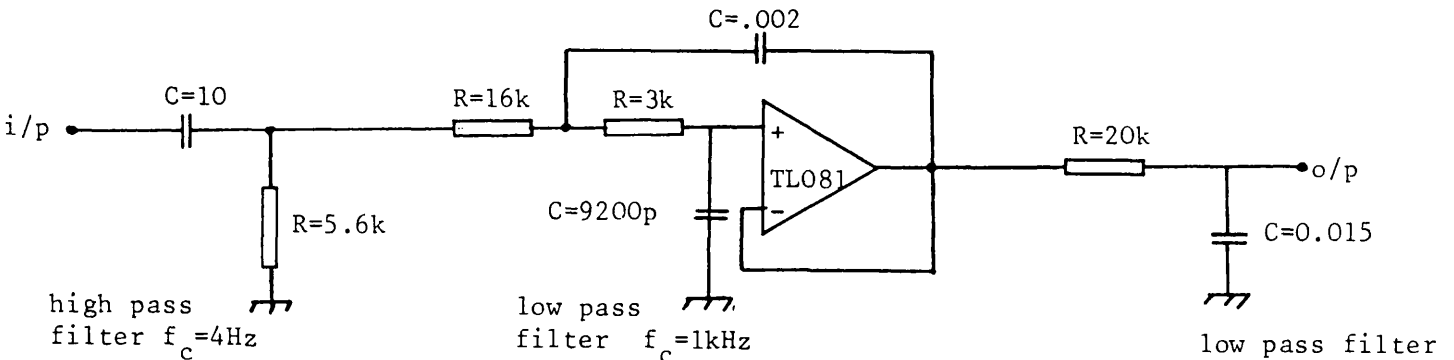


Fig. 8.4 : FIR filter output filtering circuits

All resistors are in Ω unless otherwise specified
All capacitors are in μF unless otherwise specified

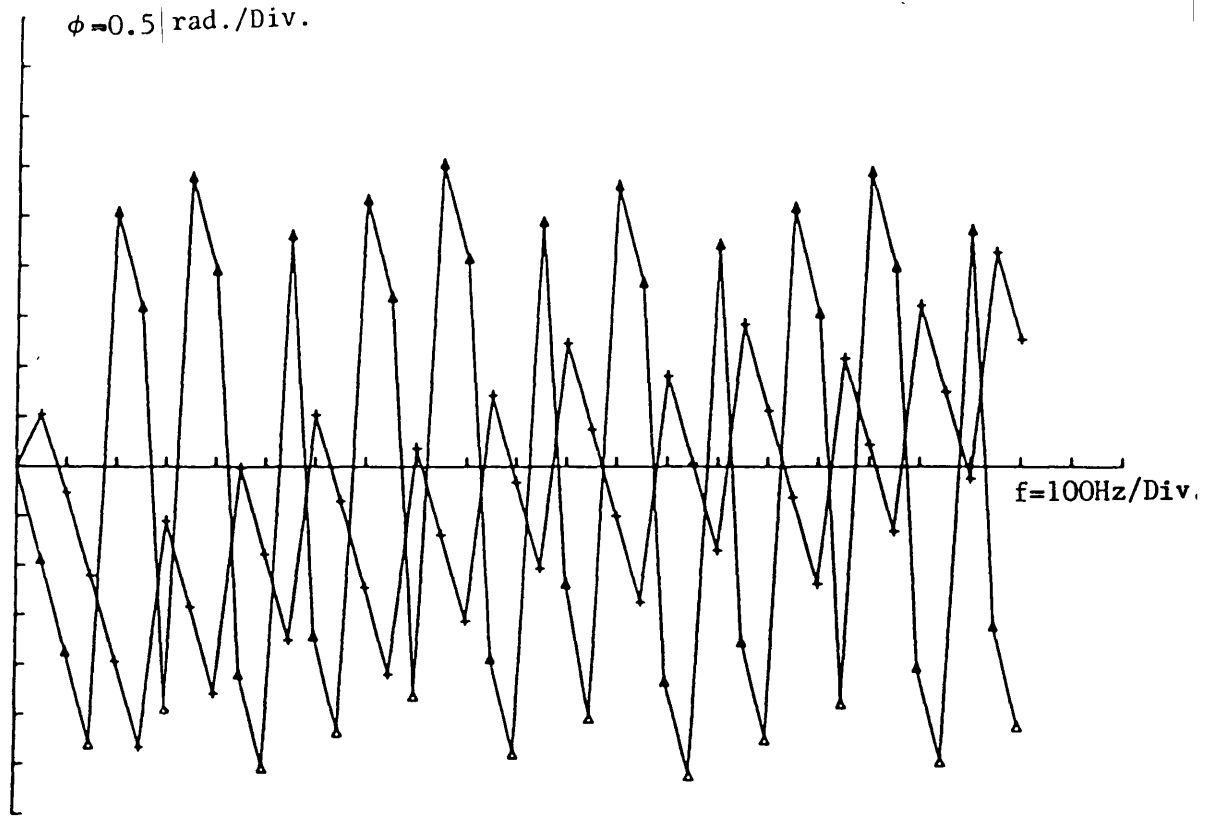


Fig. 8.5: The 6ms transformation filter impulse responses.
Cosine transformation phase response
Sine transformation phase response

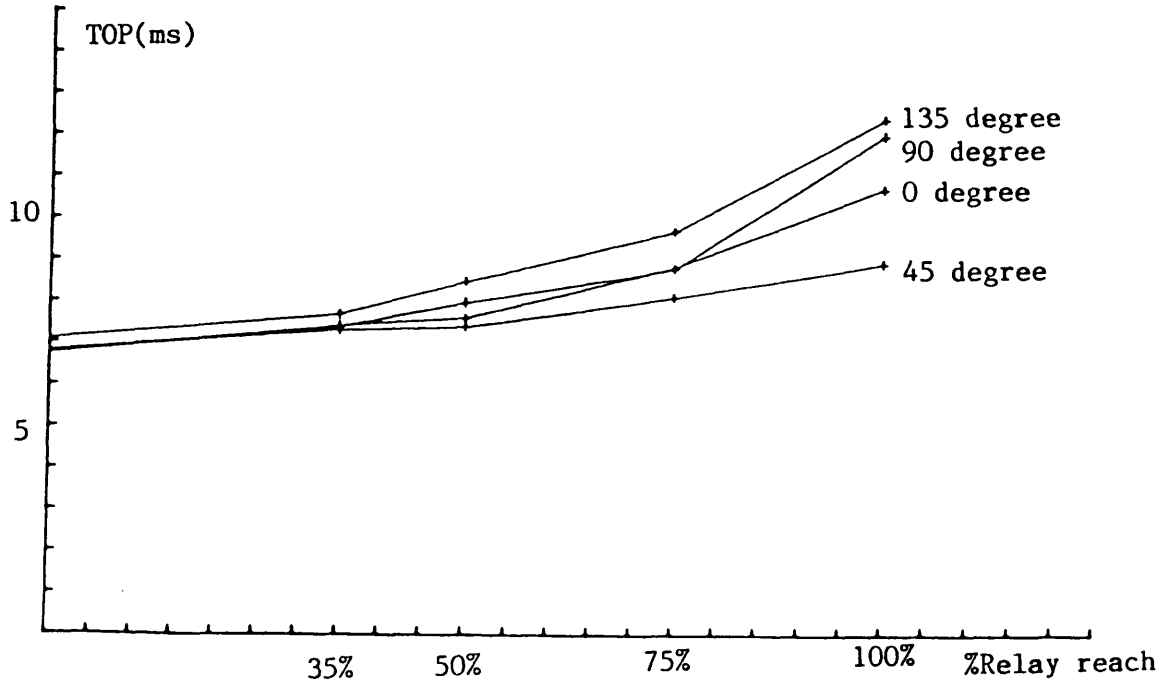


Fig. 8.6: Relay operating time versus fault distance at specific inception angles, 5 GVA source capacity at the relaying end, fault inception angles are 0, 45, 90 and 135 degrees. Lumped parameter model.

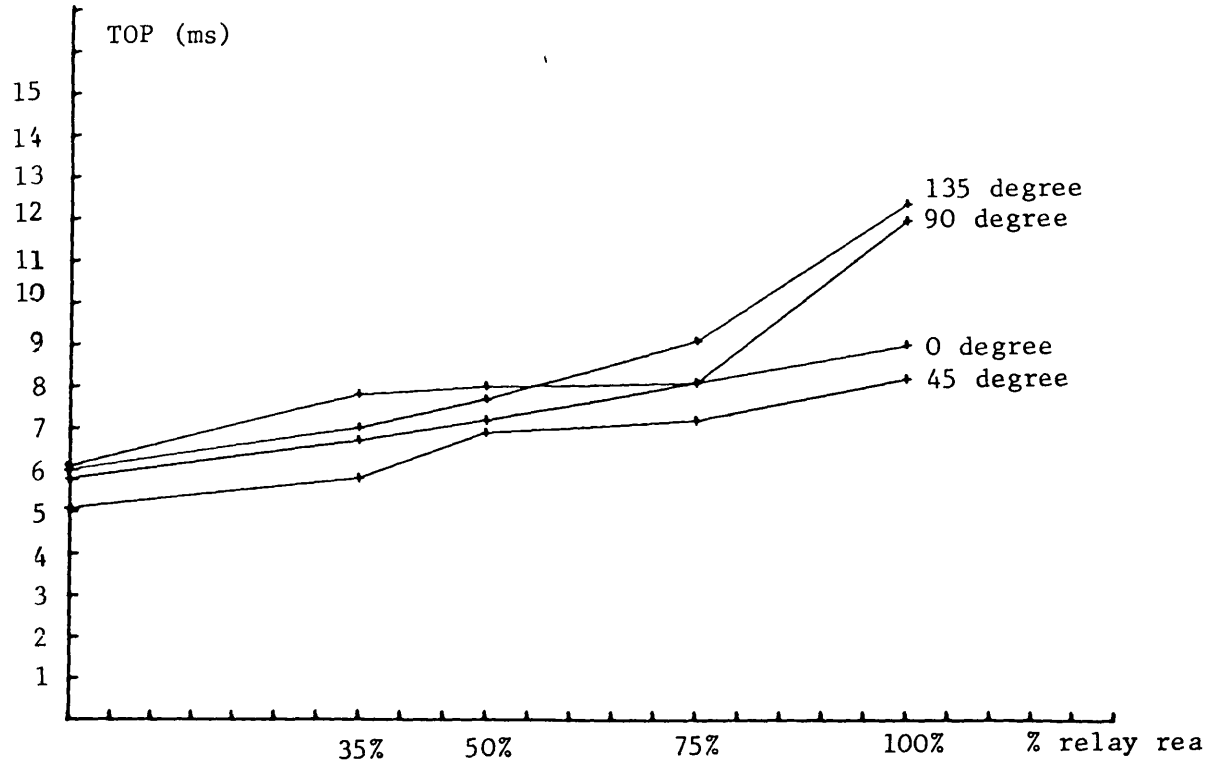


Fig. 8.7 : Relay operating time versus fault distance at specific inception angle, using lumped parameter model, 35 GVA source capacity at the relaying end. Fault inception angles are 0, 45, 90 and 135 degrees

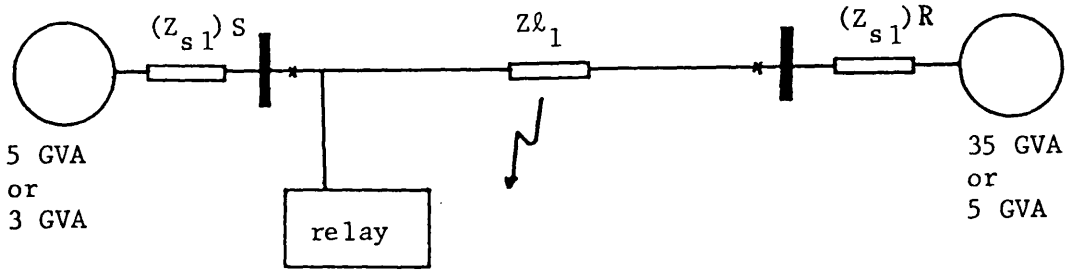


Fig. 8.8 : Double end fed, 3 phase transmission line model, phase "a-e" representation

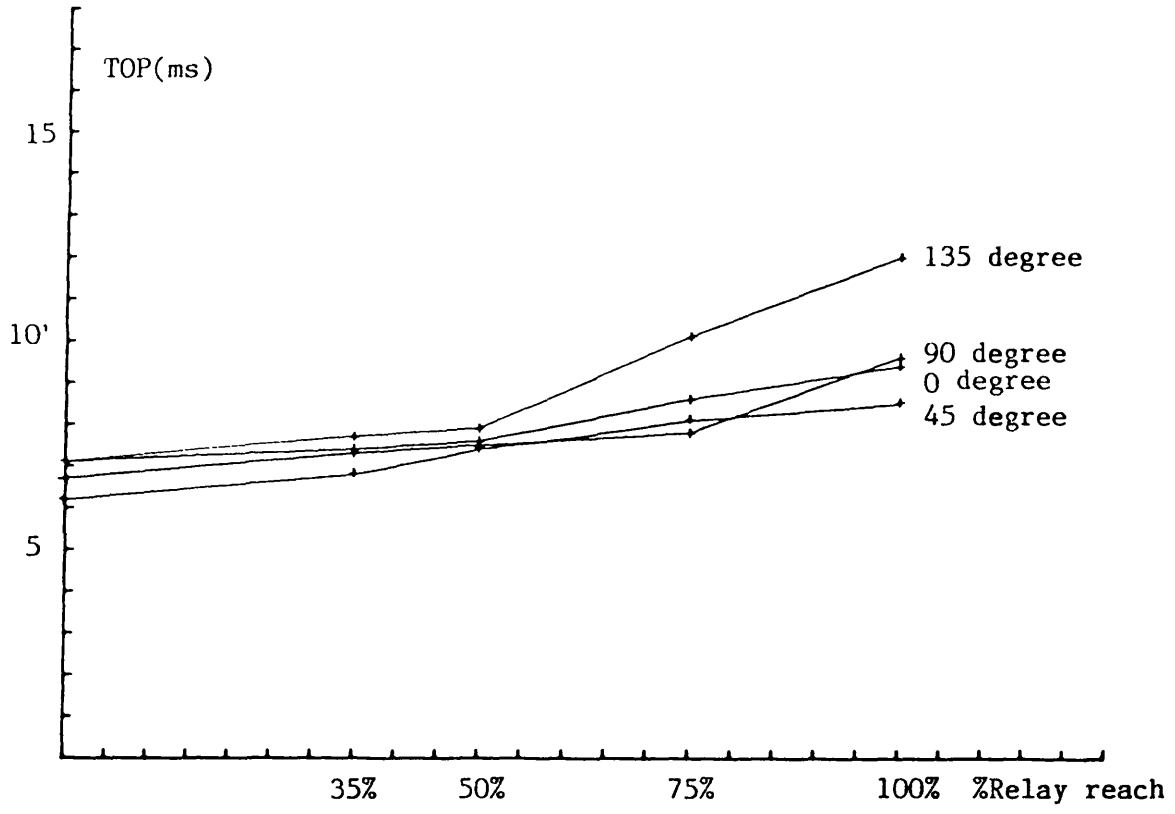


Fig. 8.9: Relay operating time versus fault distance at specific inception angles. Fault inception angles are 0, 45, 90 and 135 degrees. Lumped parameter model.

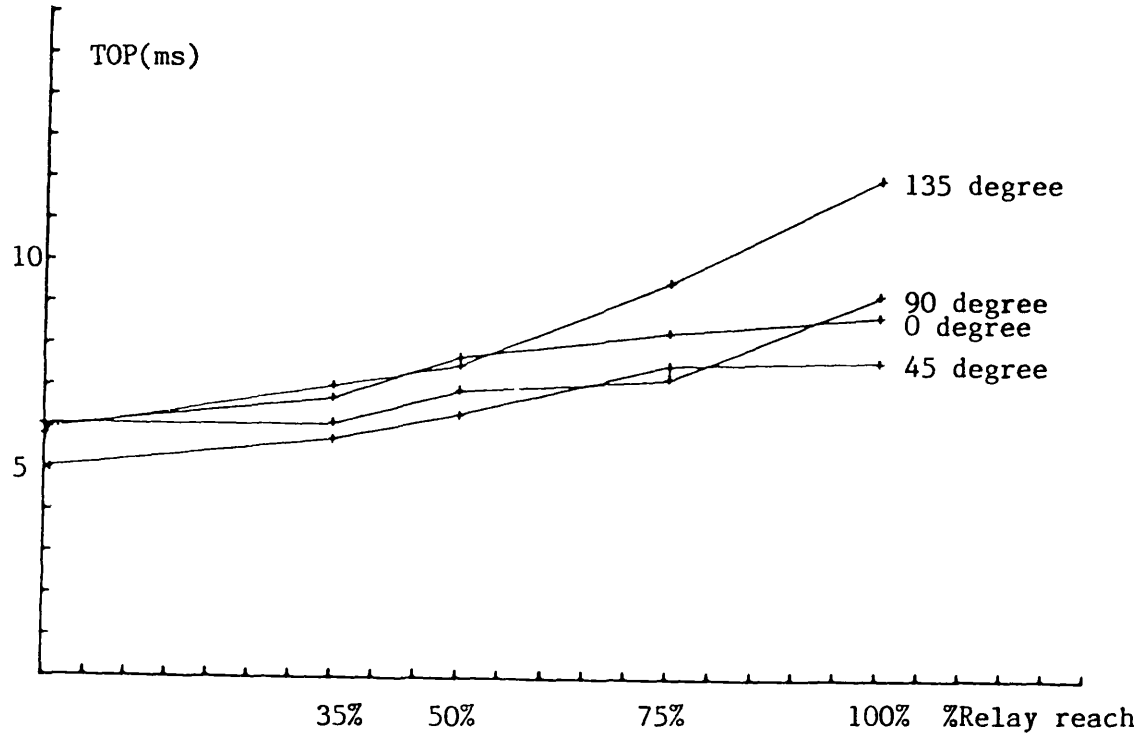


Fig.8.10: Relay operating time versus fault distance at specific inception angle. Source capacities of 35 GVA at the relaying end and 5 GVA at the remote end of the line.

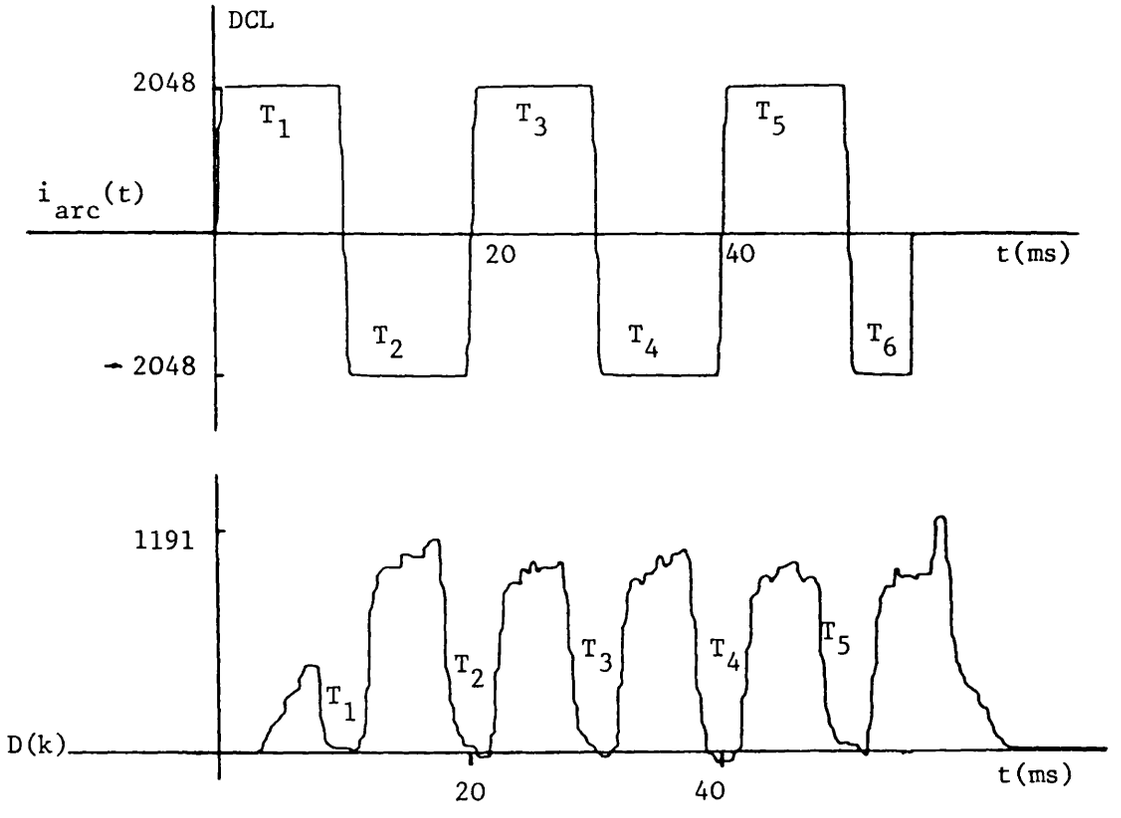


Fig. 8.11 : The response of D(k) to the relaying current clipping. 35 GVA source capacity at the relaying point, 5 GVA source capacity at the remote end, response is for solid "a-e" fault, 90 degree conception angle close-up fault. T_1, T_2 ... are the current clipping period and its impact on the relaying term D(k).

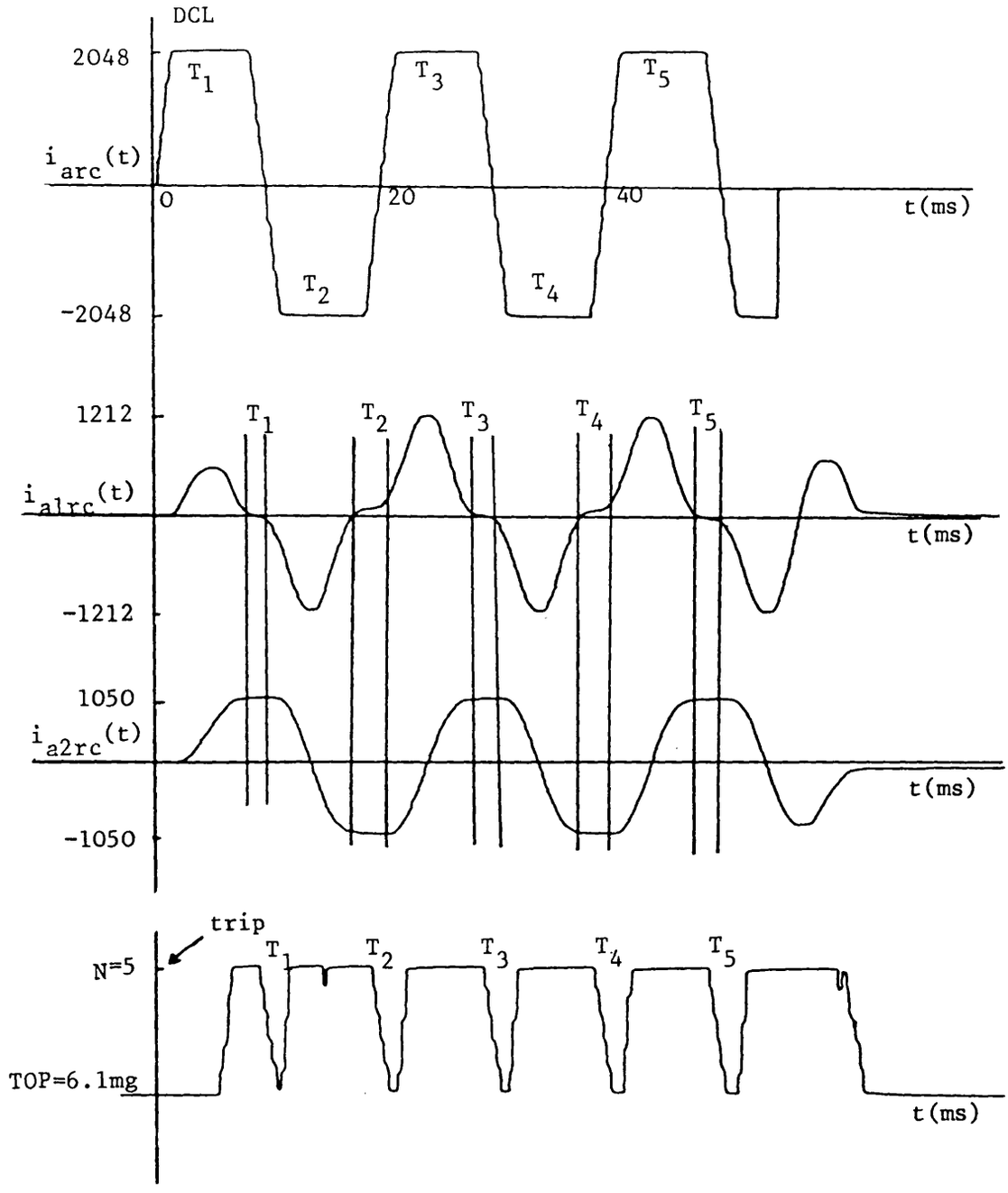


Fig. 8.12 : Decision logic counter response to relaying current clipping. 35 GVA source capacity at the relaying end, 5 GVA source capacity at the remote end. Fault at 35 km from the relaying, 90 degree inception angle. T_1, T_2 ... are the current clipping and their impact on the current transformed components and the decision logic counter.

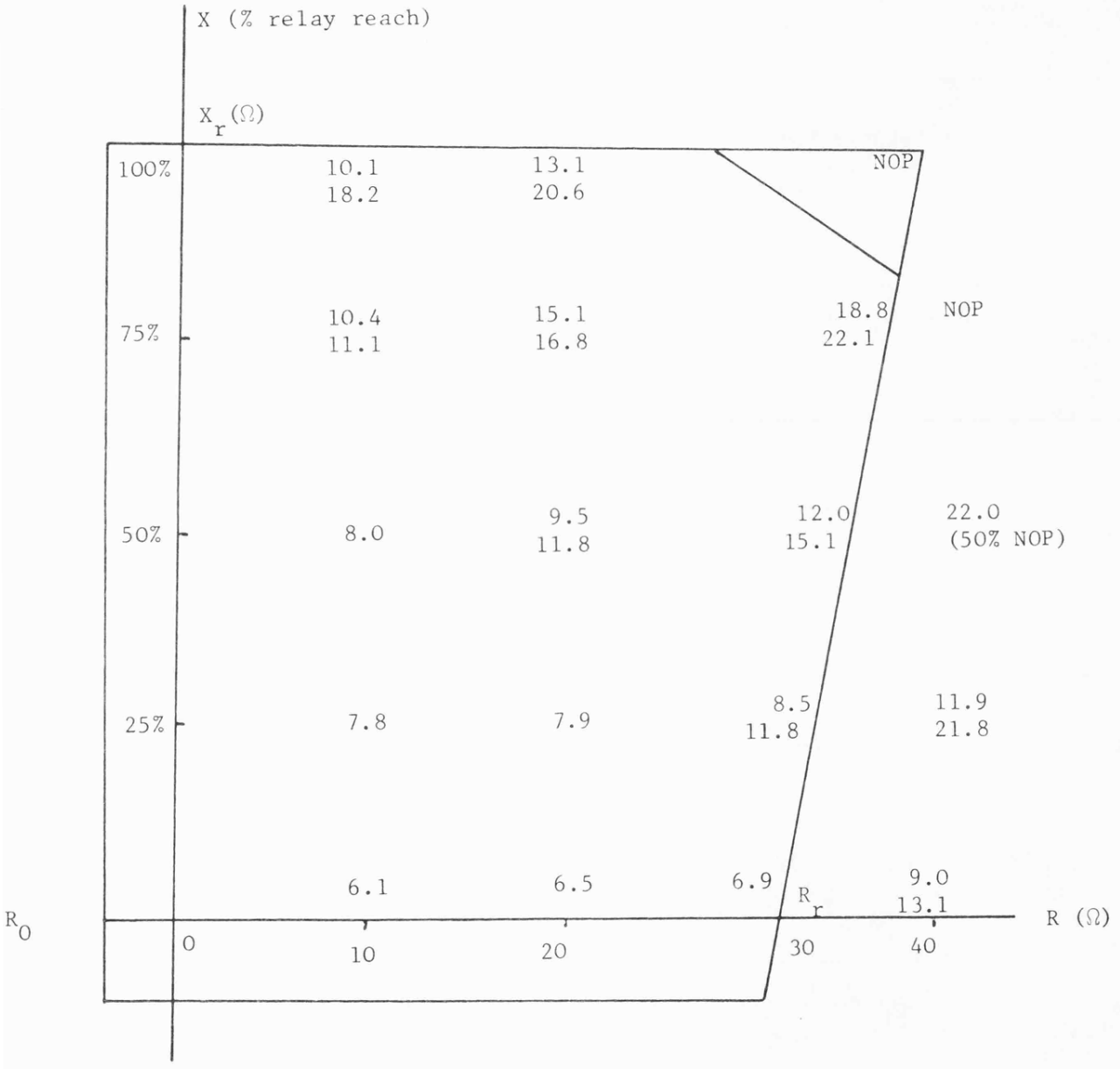


Fig. 8.13a: Relay operating time for specific resistive faults, 0 degree inception angle. 35 GVA source capacity at the relaying end and 5 GVA source capacity at the remote end.

* The two operating times for some resistive faults represent the max. and min. operating time.

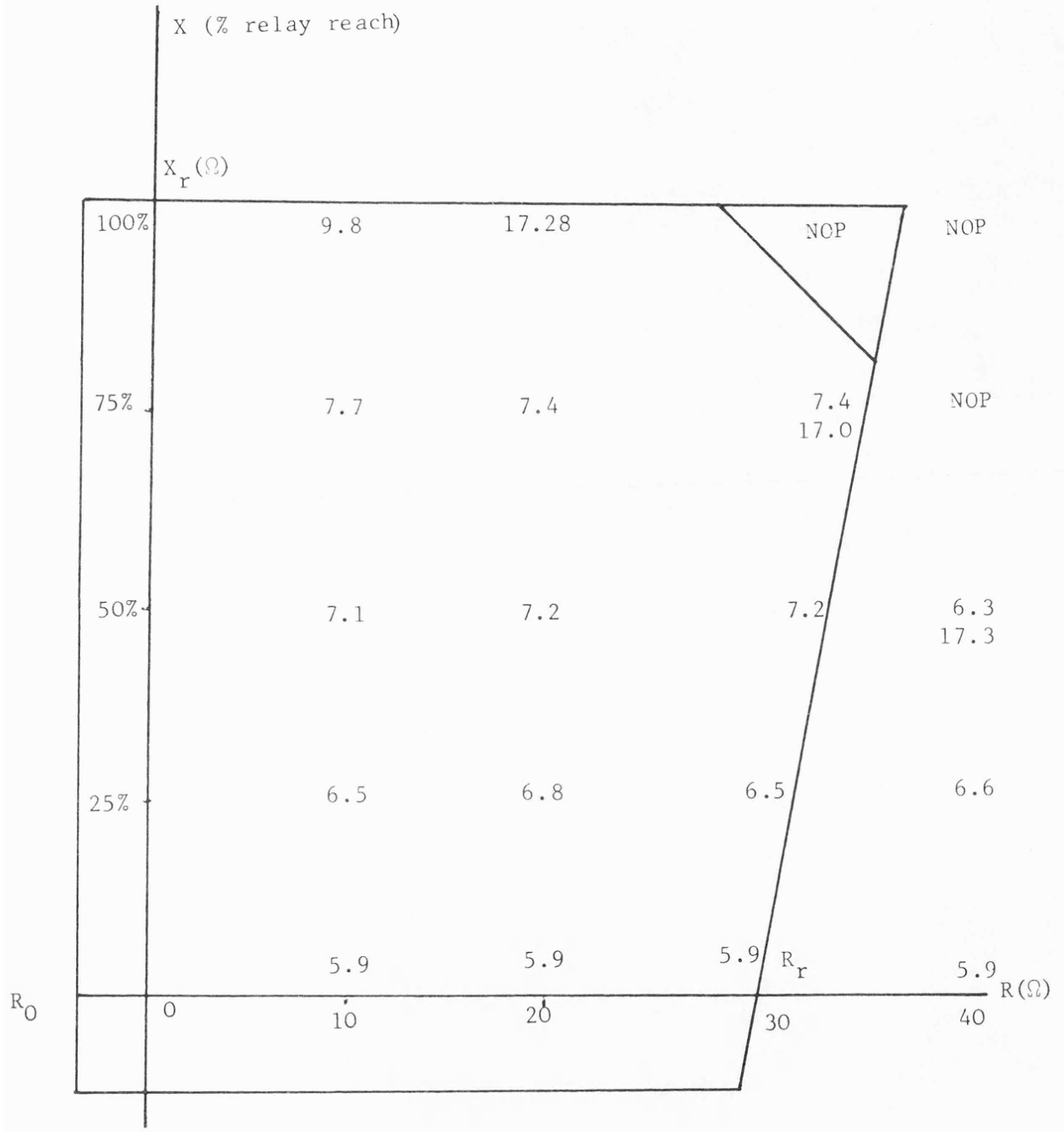


Fig. 8.13b : Relay operating time for specific resistive faults, 90 degree inception angle. 35 GVA source capacity at the relaying end and 5 GVA source capacity at the remote end.

*The two operating time for some resistive faults represent the max. and min. operating time.

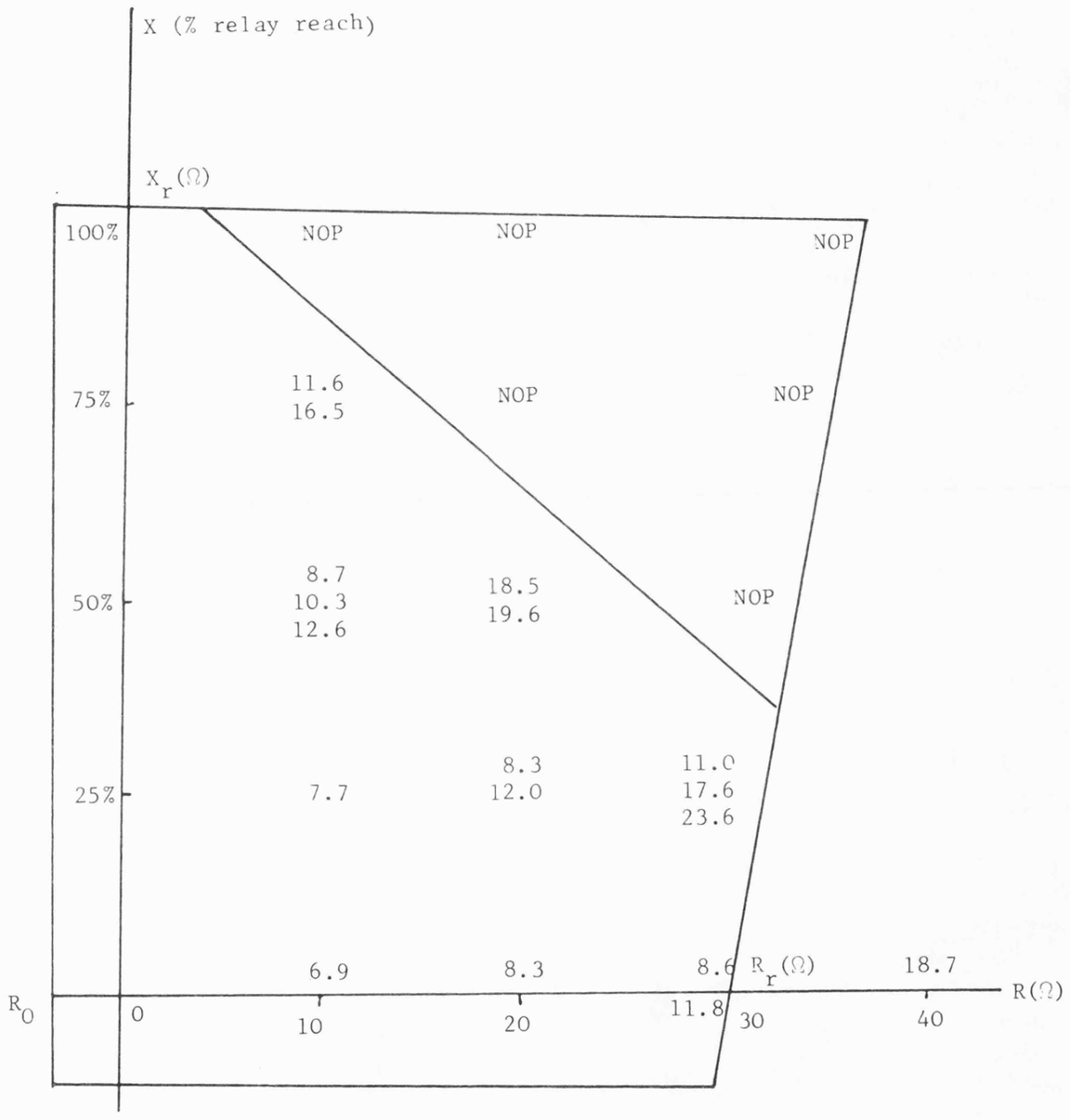


Fig. 8.13c : Relay operating time for specific resistive faults, 0 degree inception angle. 5 GVA source capacity at the relaying end and 35 GVA source capacity at the remote end.

*The two operating time for some resistive faults represent the max. and min. operating times.

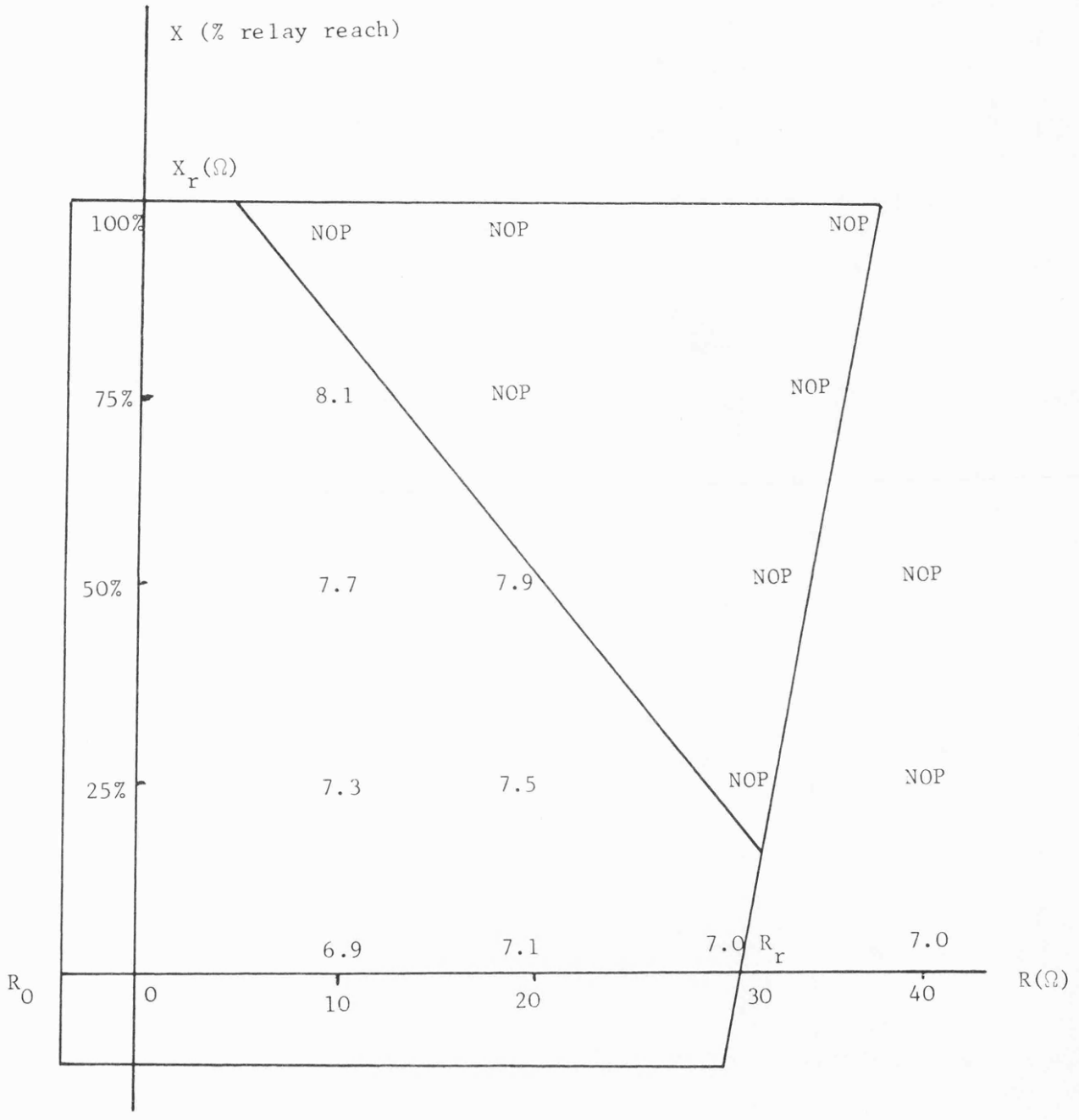


Fig. 8.13d : Relay operating time for specific resistive faults, 90 degree inception angle. 5 GVA source capacity at the relaying end and 35 GVA source capacity at the remote end.

*The two operating time for some resistive fault represent the max. and min. operating time.

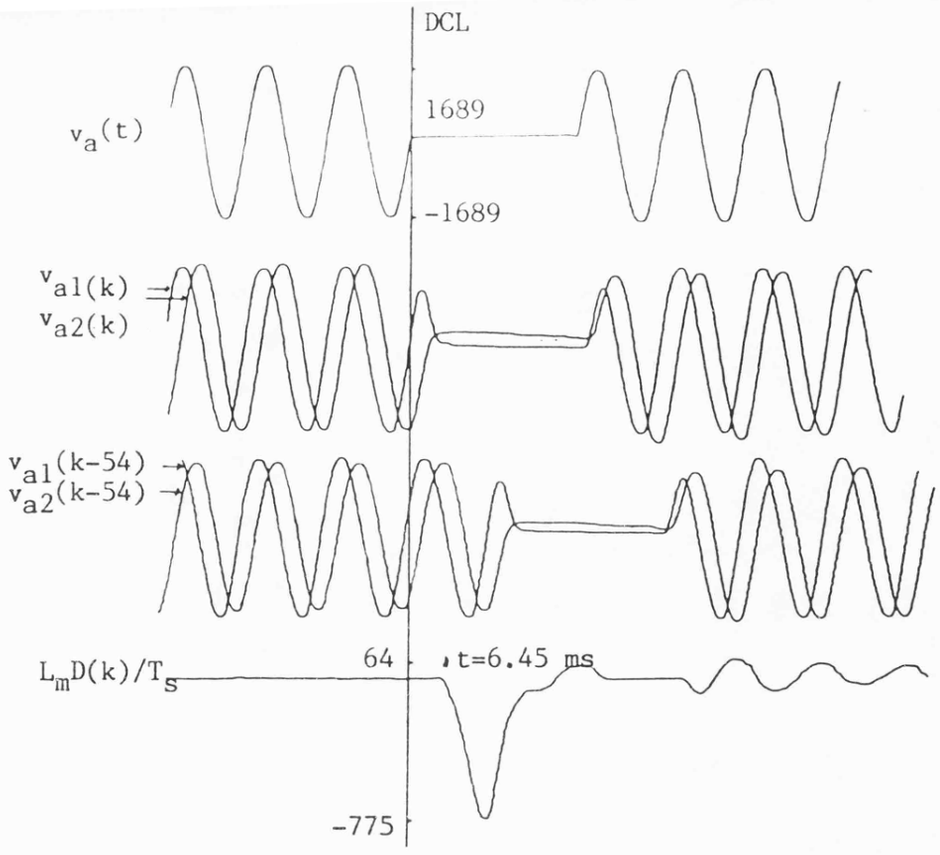


Fig. 8.14a: The behaviour of the term $L_mD(k)/T_s$ for 0 degree inception angle close-up fault, 5GVA capacity at the relaying point.

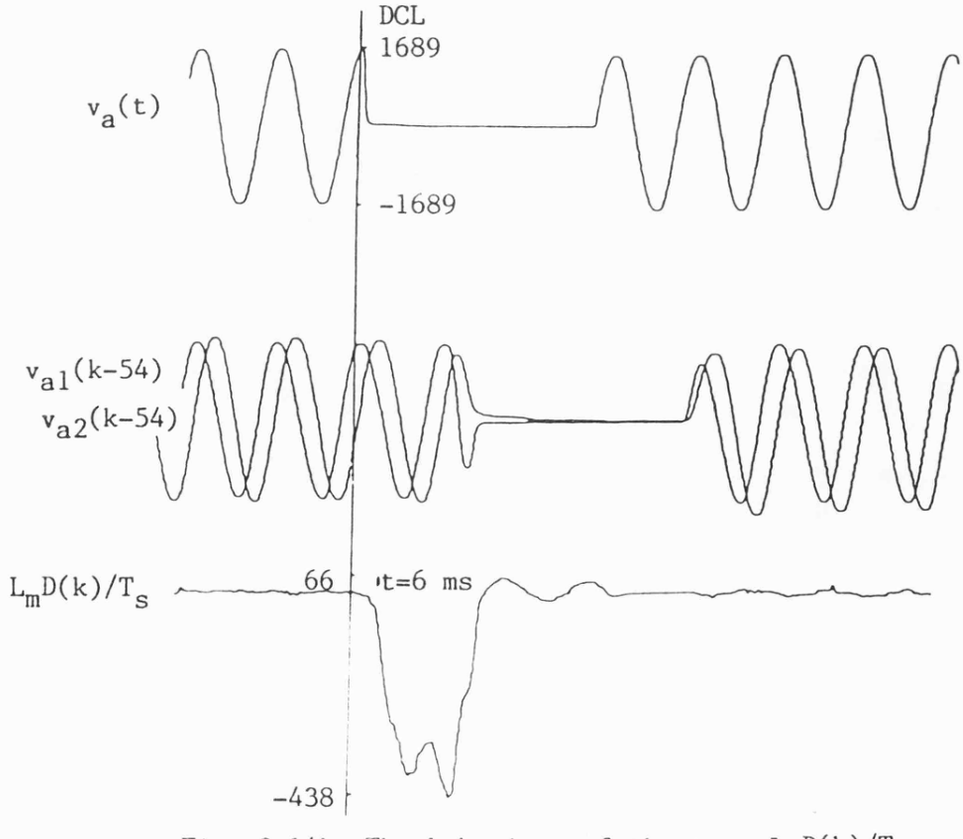


Fig. 8.14b: The behaviour of the term $L_mD(k)/T_s$ for 90 degree inception angle fault, 5 GVA capacity at the relaying point.

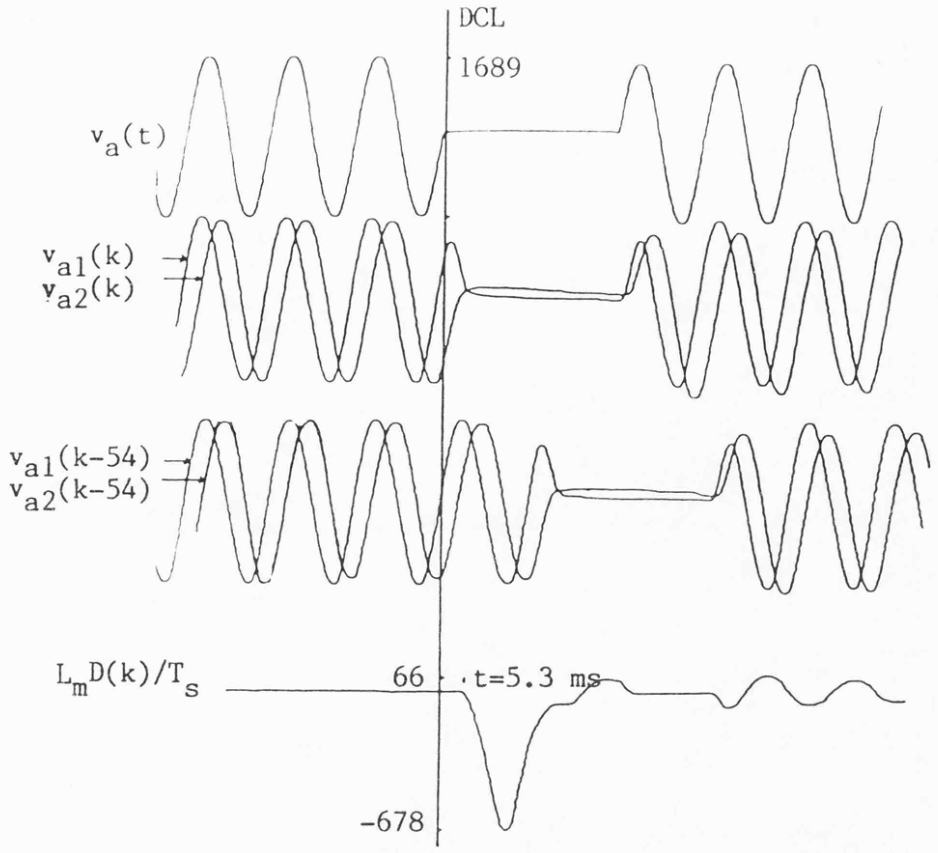


Fig. 8.14c: The behaviour of the term $L_m D(k)/T_s$ for 0 degree inception angle reverse close-up fault, 35 GVA capacity at relaying point.

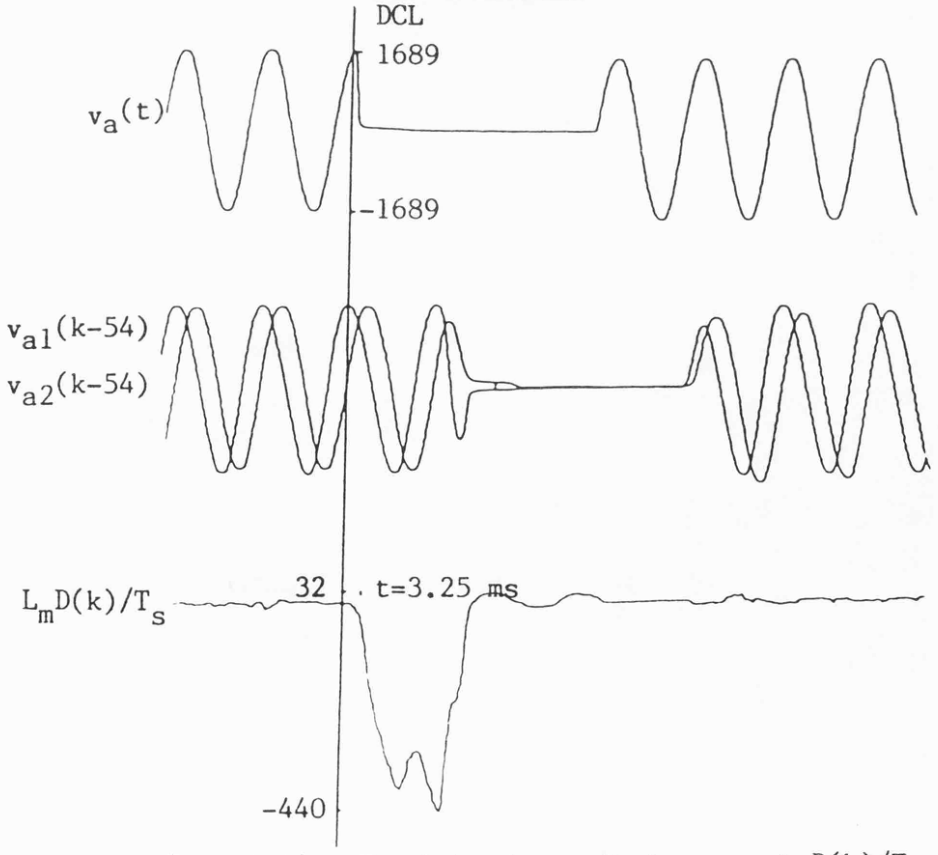


Fig. 8.14d: The behaviour of the term $L_m D(k)/T_s$ for 90 degree inception angle reverse close-up fault, 35 GVA capacity at the relaying point.

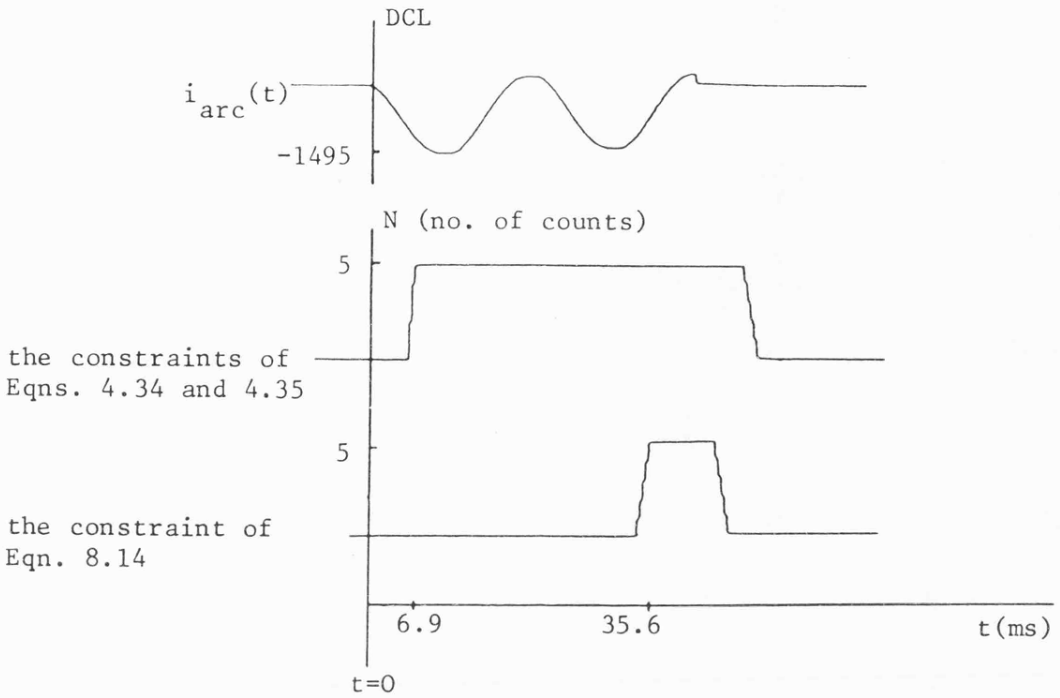


Fig. 8.15a : Decision logic counter behaviour in the event of reverse close-up fault for 0 degree inception angle, 5 GVA source capacity at the relaying end

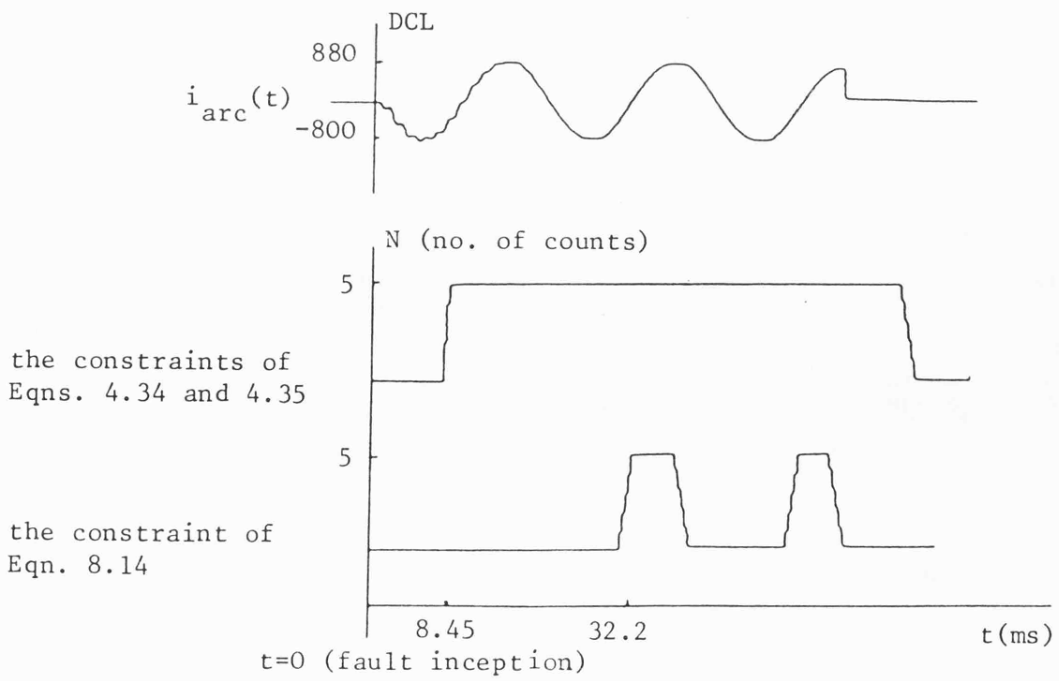


Fig. 8.15b : Decision logic counter behaviour in the event of reverse close-up fault for 90 degree inception angle, 5 GVA source capacity at the relaying end

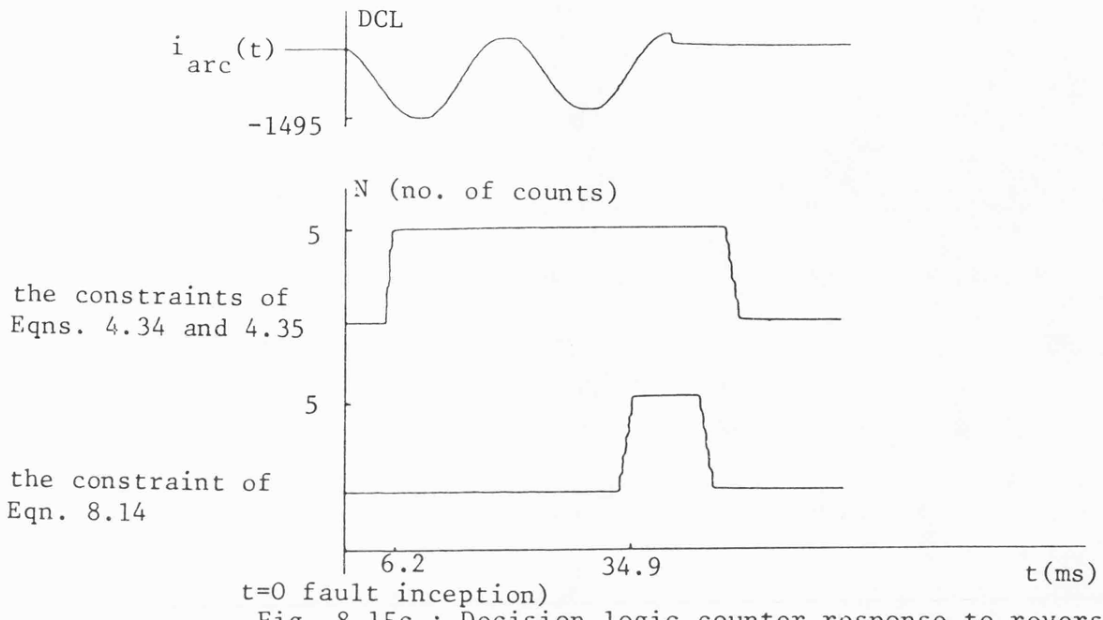


Fig. 8.15c : Decision logic counter response to reverse close-up fault for 0 degree inception angle, 35 GVA source capacity at the relaying end

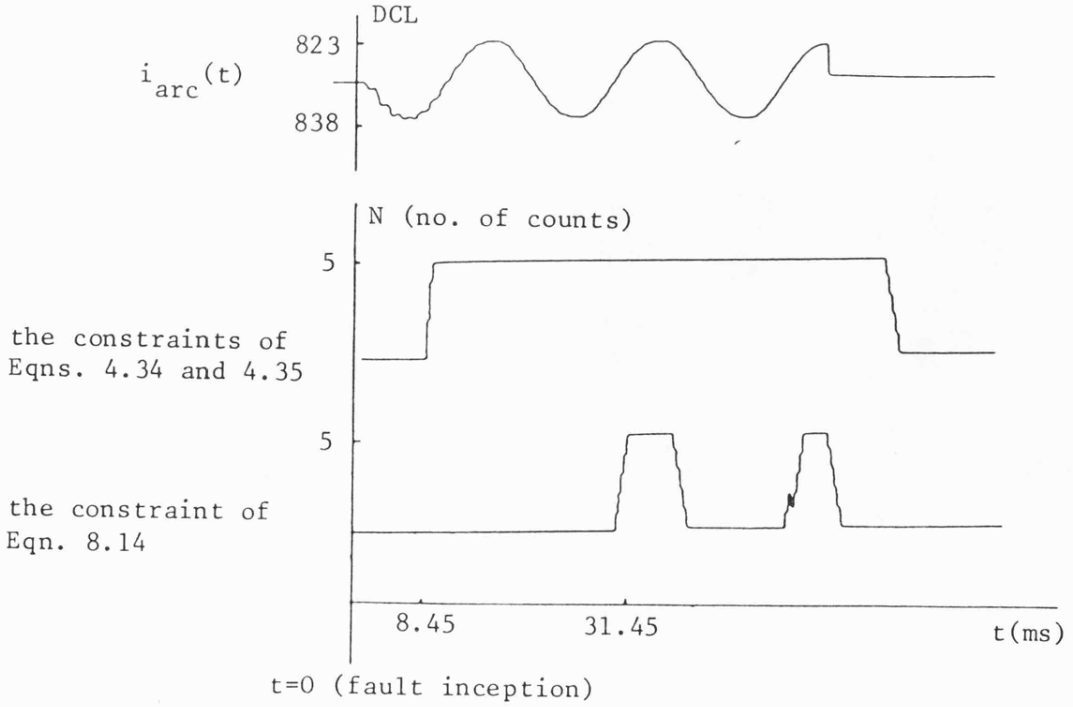


Fig. 8.15d : Decision logic counter response to reverse close-up fault for 90 degree inception angle, 35 GVA source capacity at the relaying end

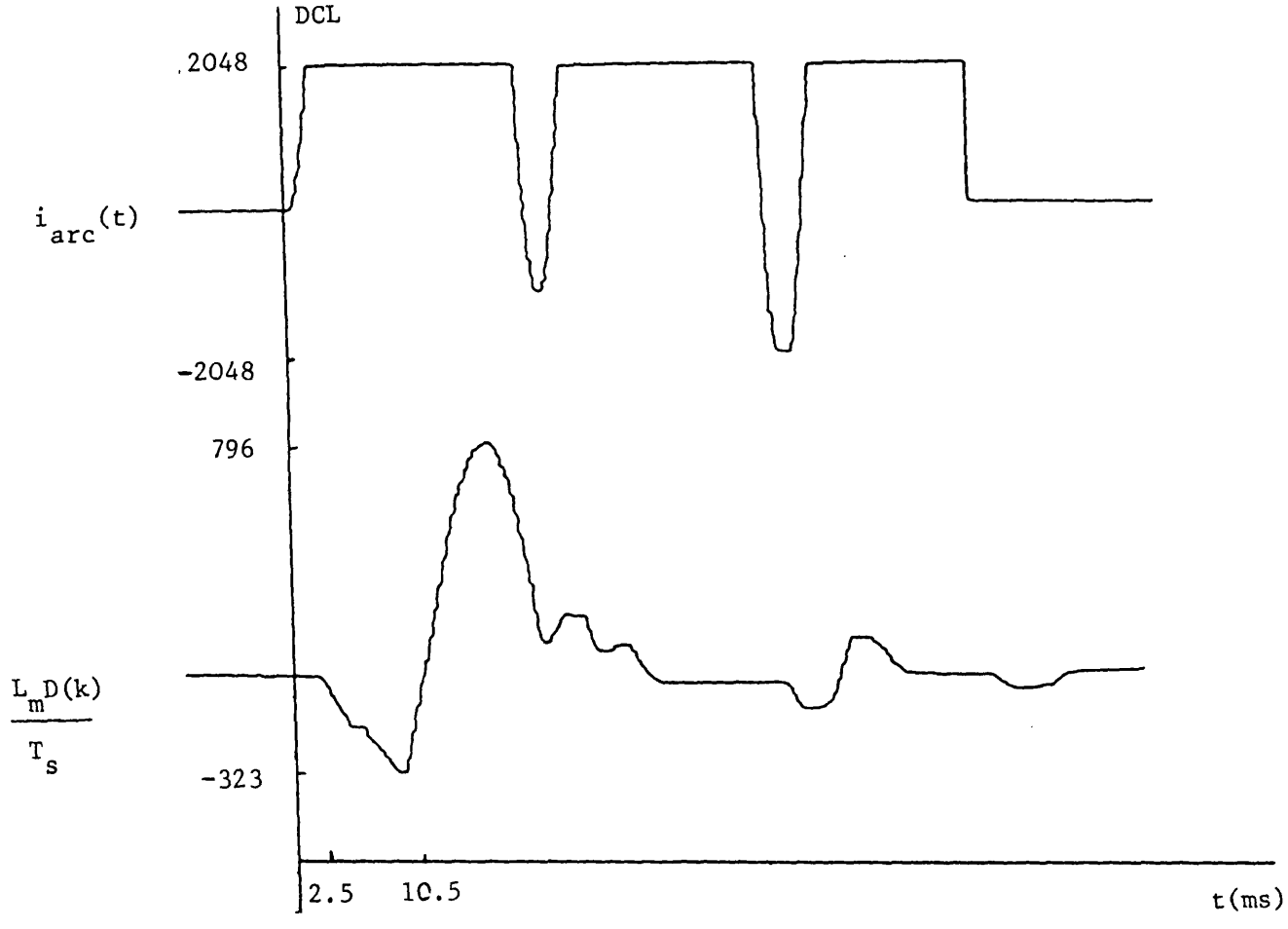


Fig. 8.16 : Response of the term $L_m D(k)/T_s$ for forward close-up fault, 35 GVA source capacity at the relaying end, 0 degree inception angle

CHAPTER 9

SHORT TRANSFORMATION WINDOW TEST

9.1 INTRODUCTION

Circuit breaker technology has advanced to the stage where 12 ms breaker opening time can be achieved, which means that a trip initiation must be accomplished in less than 4.7 ms, to achieve one cycle fault clearance, for 60 Hz system. In order to achieve such a speed, it is necessary to use a smaller transformation window than 6 ms, since the latter is not capable of meeting the one cycle fault clearance requirement. As pointed out in Chapter 4, the transformation window in theory is arbitrary, and a 2 ms transformation window was chosen to implement the scheme (f_e = 277 Hz). The relay performance is tested using the four constraints given in Chapter 4, for 128 km and 24 km lines.

9.2 FILTER IMPULSE RESPONSES

The filter coefficients $h_{1(n)}$ and $h_{2(n)}$ are obtained by using Eqns. 8.2 and 8.3, which can be expressed as:

$$h_{1(n)} = \text{COS}(n\omega_e T_s) \qquad \text{--- 9.1}$$

$$h_{2(n)} = \text{SIN}(n\omega_e T_s) \qquad \text{--- 9.2}$$

where the limits on n are from 0 to 5 and the angular extraction frequency (ω_e) is 1413.716 rad/sec for a 2.7 kHz sampling rate. Fig. 9.1 shows the filter coefficients and Fig. 9.2 shows the CCD filter impulse responses, obtained by injecting a pulse at a period greater than the window width T_w.

As the relaying voltage and current filter impulse responses are adjusted individually, there is the possibility of a small error between similar impulse responses. For example, a steady state input to the filters used to derive $v_1(t)$ and $i_1(t)$ shows a small variation in the phase shift between the cosine filter outputs. In order to eliminate this error, the outputs of two similar filters were fed to the terminals input of a differential amplifier and the coefficients of one of the filters were finely adjusted to match its equivalent, such that the output of the differential amplifier is zero.

9.3 RELAY NOISE IMPACT ON SHORT DATA WINDOW

Initial tests show a considerable noise content in the FIR filters output signals as shown in Fig. 9.3, for the cosine transformation filter. The noise appearing in the filter output is from two sources:

1 - Relay power supply noise, Fig. 9.3, which can be eliminated by using separate power supplies for the CCD filters.

2 - CCD input gate protection diodes, Fig. 9.4, which can be eliminated by removing the protection diodes.

Fig. 9.4a shows the FIR filters output with separate power supplies and without the protection diodes. In this respect, it must be noted that the 6 ms transformation window is capable of filtering the supply and diode noise components, whereas these noise sources become apparent with the use of the 2.2 ms window.

9.4 FILTER FREQUENCY RESPONSES

Fig. 9.5 shows the filter simulated frequency responses. The first zero of the frequency response, with more than 22.27 dB and 33.9 dB attenuation for the cosine and sine filters, occurs at 700 Hz. This is more

appropriate when compared with the 6 ms transformation in which the first zero occurs at 250 Hz, since the fault induced travelling wave is approximately 900 Hz for a fault at 102 km from the relaying end. However, it can be seen that the side lobes for the 2.2 ms transformation window are larger when compared to those of the 6 ms transformation window, which inevitably makes the decision logic process mor susceptible to noise. Fig. 9.6 shows the CCD filter measured frequency responses.

9.5 FILTER PHASE RESPONSE

Fig. 9.7 shows the filter phase response. The phase shifts of the two filters can be obtained from Fig. 9.7 as:

$$T_d(\omega)/\omega=\omega_0 = \frac{d\phi_{11}}{d\omega} - \frac{d\phi_{12}}{d\omega} = 2.54 \text{ ms} \qquad \text{--- } 9.3$$

where ϕ_{11} and ϕ_{12} are the phase shift of the filters $H_1(\omega)$ and $H_2(\omega)$ at frequency f_0. The phase shift of 45 degrees is identical to the measured phase shift at 50 Hz.

As shown in Appendix 3, the relaying term D(k) for a steady state sinusoidal input is given by Eqn. A3.16, which takes the form:

$$D_{ss} = |H_1(\omega_0)||H_2(\omega_0)| \; I_p^2 \; \text{SIN}(\phi_{11}-\phi_{12}) \; \text{SIN}(\omega_0 T_s) \qquad \text{--- } 9.4$$

For a phase shift of 45 degrees, the D_{ss} magnitude is attenuated by 29%, compared with 2% attenuation in D_{ss} magnitude for a 6 ms transformation window. Therefore under small signal conditions, the relaying term D(k) is less immune to noise.

9.6 RELAY TEST

The 2.2 ms transformation window was tested for a 128 km, double end fed three phase system. The test is performed for 0 and 90 degree inception angles. The fault distance were 0.35%, 50%, 75%, 100% of the relay reach. For the SIR test, a shorter line was chosen (24 km).

9.6.1 Case 1 : 5 GVA Source capacity at the relaying end and 35 GVA source capacity at the remote end

Fig. 9.8 shows the relay operating time for 0 and 90 degrees fault inception angles. The minimum operating time is achieved for a close-up fault (4.4 ms). As the fault distance is increased, the relay response becomes progressively slower. The slowest operating time for faults up to 75% of the relay reach is 7.2 ms.

9.6.2 Case 2 : 35 GVA Source capacity at the relaying end and 5 GVA source capacity at the remote end

Fig. 9.9 shows the relay performance for 0 and 90 degrees inception angles. Once again, the fastest operating time is for close-up fault (3.8 ms), whilst the slowest operating time for a fault at 75% of the relay reach is 7.2 ms.

9.7 SIR TEST

For practical considerations, the SIR test is performed using a short line, since high SIR is associated with a small line impedance. In order to test the relay performance for various SIR, a 24 km line was chosen ($Z\ell_1$ = 5.51 Ω for a fault at 100% of the relay reach, 19.2 km). The relay is tested for SIRs of 4.6, 11.6, 17.8 and 23 which correspond to 5, 2, 1.3 and 1 GVA source capacities at the relaying end. The

relay operating time is obtained for faults at 0%, 50%, 75% and 100% of the relay reach. The fault data is obtained using the primary system simulation [6].

9.7.1 Case 1 : Relay operating time against fault location for a given SIR and 90 degree inception angle

Fig. 9.10 shows the relay operating time for a given SIR. The fastest operations were achieved for a SIR of 4.6. The relay operating time increased for higher SIRs.

9.7.2 Case 2 : Relay operating time against fault location for a given SIR and 0 degree inception angle

Fig. 9.11 shows the relay operating time for a given SIR. The operating time characteristic is observed to be similar to that of Section 9.7.1.

9.7.3 SIR test assessment

The SIR tests confirm the general trend of the relay performance, where the relay operating time increases as SIR increases. In this respect it must be noted that the increase in the relay operating time is due to two factors:

1 - The noise content of the signals. As the signals become smaller, the noise plays a more dominant role in dictating the relay operating time.

2 - The transient nature of the measurands in the immediate post fault period.

Comparing Figs. 9.10 and 9.11, it can be clearly seen that the relay operation is faster for 0 degree inception angle, for a given SIR and fault location.

9.8 RELAY REACH ACCURACY TEST

The 2.2 ms transformation window reach accuracy confirmed the conclusion that smaller data windows are susceptible to noise. The reach accuracy is investigated for 128 km and 24 km lines. For the 24 km SIR values of 4.6, 11.6, 17.8 and 23 which correspond to source capacities of 5, 2, 1.3 and 1 GVA at the relaying end, were investigated. Faults beyond the relay reach were simulated by increasing the relaying voltage for a fault at 100% of the relay reach. For the 128 km line and 90 degree inception angle, a 5% accuracy reach is achieved, for both 5 and 35 GVA source capacities at the relaying end. A similar reach accuracy is achieved for 0 degree inception angle and 5 GVA source capacity at the relaying end. However, for 0 degree inception angle and 35 GVA source capacity, a 15% overreach is observed. For the 24 km line, it was observed that considerable overreach occurred at high SIR. For example, at an SIR of 7.7, 90 degrees inception angle, an overreach of over 20% could sometimes be observed. For 0 degree inception angle, the relay overreach is further aggravated.

9.9 RELAY OVERREACH ASSESSMENT

The considerable relay overreach is due to two factors, relay noise and the sinusoidal component of D(k) due to the relaying current exponential offset.

9.9.1 Case 1 : 90 degree inception angle overreach analysis

Consider the relaying term D(t), which is given by Eqn. 4.15 as:

$$D(t) = i_1(t)\, i_2'(t) - i_1'(t)\, i_2(t) \qquad \text{--- } 9.4$$

The current differential terms $i_2'(t)$ and $i_1'(t)$ can be expressed in

discrete form as:

$$i'(k) = 1/T_s \left(i(k) - i(k-1)\right) \qquad \text{--- } 9.5$$

The relay noise has a particular effect on the relaying term D(k), since noise accentuates errors due to differencing. Fig. 9.12 shows D(k) for a fault at 100% of the relay reach (19.2 km) from the relaying end, SIR of 4.6. With respect to Fig. 9.12a, it can be seen that the maximum variation due to noise is near the current peak, where the rate of change is minimum. Fig. 9.12b shows the filtered version of D(k), where an external low pass filter with a 500 Hz cut-off frequency is used. Fig 9.12b shows that D(k) magnitude is in the order of 20 digital conversion level (DCL). However, the maximum variation in the relaying term D(k) as shown in Fig. 9.12a is (+ and - 14 DCL). The effect of D(k) noise on the decision logic counter is shown in Fig. 9.13 for a fault 10% beyond the relay reach, for SIR of 4.6, where a random trip signal can be initiated (most probably near the peaks).

9.9.2 Case 2 : 0 degree overreach analysis

As described in Section 4.4, the relaying term D(k) is sensitive to the exponential offset relaying current. For a pure sinusoidal input, D(k) has a d.c. magnitude. In the event of an exponential offset, D(k) develops a sinusoidal component, imposed on the steady state d.c. level. Under strong exponential offset condition, the determinant term sinusoidal component can achieve a negative value, thus the constraints involving D(k) are not satisfied. In order to ensure that D(k) is unipolar, the exponential offset has been reduced using a high pass filter with 4 Hz cut-off frequency. It has been found that reducing the exponential offset by less than about 50% maintains a unipolar D(k) level,

thus providing a stable solution to the algorithm [4, 19]. Although the reduction of the exponential offset provides a stable solution, however it produces an overreach problem. Consider the constraint $LD(k)/T_s < K_4\ D(k)$. As D(k) develops a sinusoidal component in the event of the relaying current exponential offset, $LD(k)/T_s$ should develop a similar sinusoidal component, in phase and magnitude, thus the measured reactance should not be in error. However, test has revealed that this is not the case as shown in Fig. 9.14. With reference to Fig. 9.14, the relaying term $LD(k)/T_s$ reaches minimum values at points B and D in 20 ms intervals, while the term D(k) reaches a minimum value at point F in 23 ms. The magnitude of the peak to peak of the sinusoidal component (point A to B) for $LD(k)/T_s$ is 8.4 and for D(k) (point E to F) is 4.1, which indicates that the relative magnitude of the sinusoidal component is not the same, due to an error component introduced by the exponential offset of the relaying current signal. For a fault just beyond the relay reach, the decision logic counter response to a fault at 20 ms intervals, coincide with the reduced level of $LD(k)/T_s$ and D(k). Fig. 9.15a shows the behaviour of D(k), 0 degree inception angle for SIR of 4.6 and Fig. 9.15b shows the response of the decision logic counter. It has been observed that the magnitude of the downward droop in the measured impedance which causes the decision logic counter to be incremented at 20 ms intervals is directly proportional to the exponential offset. For example, if the first occurring of up counting cause 20 increments then the increments in the following occurrence is approximately 1/3 of that if the first, i.e. about 7 counts.

9.10 RELAY OVERREACH PRACTICAL CONSIDERATIONS

From the observations outlined in Sections 9.9.1 and 9.9.2, the following

practical considerations are accomplished:

1 - A better realization of the FIR filter hardware structure, with improved signal to noise ratio, such as 12-bit digital FIR filters.

2 - The filters must be capable of eliminating the exponential offset of the relaying current signals, since reducing the exponential offset produces a considerable relay overreach.

9.11 PHASE MODIFIED FINITE FOURIER TRANSFORM PROCESS

In order to improve the relay performance at low level signal conditions, the sine and cosine convolution filters are modified, such that the filters phase shift is 90 degrees. This will prevent any attenuation in D(k) magnitude, thus improving the relay performance at low level signals. This requirement can be achieved by modifying the sine and cosine convolution filters such that:

1 - The sine and cosine filter impulse responses are symmetrical at the centre of the window.

2 - The peak of the sine convolution filter impulse response coincides with the zero crossing of the cosine convolution filter impulse response.

Numerically, for the 1.5 ms transformation window, the cosine filter impulse response can be obtained by evaluating Eqn. 9.5 [4]:

$$h_{1(n)} = \text{COS}(n\omega_e T_s) \qquad \text{--- 9.5}$$

where $h_{10} = -h_{15} = 1$, $h_{11} = -h_{14} = \text{COS } 1.5\ \omega_e T_s = 0.7074$, $h_{12} = -h_{13} = \text{COS } 2.5\ \omega_e T_s = 0.2607$. Similarly the sine convolution filter impulse response can be obtained by evaluating Eqn. 9.6:

$$h_{2(n)} = \text{SIN}(n\omega_e T_s) \qquad \text{--- 9.6}$$

where $h_{20} - h_{25} = \text{SIN } 0.5\ \omega_e T_s = 0.2584$, $h_{21} = h_{24} = \text{SIN } 1.5\ \omega_e T_s = 0.7063$,

$h_{22} = h_{23} = 1$. Fig. 9.16a shows the phase modified finite Fourier Transform filter impulse responses. In theory, the phase modified filters coefficients give a phase shift $(\phi_{11} - \phi_{12})$ of 90 degrees. In practice, each CCD filter is used to realize two filtering functions with one sample shift (odd and even taps are used for the cosine and the sine filters respectively), thus a filter phase shift of 74 degrees is obtained. A filter phase shift of 77 degrees represents a 3.8% attenuation in D(k) magnitude and this is insignificant when compared with 29% attenuation using the conventional Fourier Transform impulse responses (see Section 9.5).

9.12 RELAY TEST USING THE PHASE MODIFIED FOURIER TRANSFORM TECHNIQUE

The relay was tested using line configurations similar to those described in Section 9.6. With respect to the test observations described below, a preliminary D(k) threshold is set (8 digital conversion levels). The threshold is implemented such that if D(k) measurement is smaller than 8 conversion levels, the measurement is regarded unreliable and the decision logic counter is decremented.

9.12.1 Case 1 : 128 km, Double end fed line test

Fig 9.16b shows the relay operating time for 0 and 90 degrees fault inception angles. The minimum operating time is obtained for close-up fault (less than 5 ms). With respect to faults at 100% of the relay reach, relay operation is not guaranteed.

9.12.2 Case 2 : 24 km, Double end fed line test, for various SIR

Fig. 9.17 shows the relay operating time for 90 degree inception angle, with source capacities of 5, 2, 1.3 and 1 GVA at the relaying end. With

respect to Fig. 9.17, the relay maintains a consistent operation for SIR of 17.6. For SIR of 23, the relay operating time is inconsistent, which indicates that it is affected by D(k) noise threshold (see Section 9.12). For 0 degree fault inception angle, Fig. 9.18, the relay operating time increased for higher SIR, and for SIR of 23, the relay operating time was 13.2 ms for close-up fault and the relay does not operate for a fault beyond 50% of the relay reach.

9.13 RELAY REACH ACCURACY TEST

The relay accuracy reach is tested for the 128 km line and the 24 km line for various SIR. With respect to the relay accuracy test described below, only 90 degrees angle is taken, since a considerable overreach is encountered for 0 degrees inception angle. The technique for eliminating the exponential offset of the relaying current signals will be described in Section 9.16

9.13.1 128 km Line

For 90 degrees fault inception angle, using 5 GVA or 35 GVA source capacities at the relaying end, a 5% accuracy reach was observed.

9.13.2 24 km Line

For the 24 km line, the relay reach accuracy was tested for SIR of 2.5, 4.6, 5.8, 7.7, 11.6, 17.8. A relay reach accuracy of less than 9% was observed for faults up to SIR of 5.8. For a SIR of 7.7, a 17% overreach was observed and for SIR of 11.6, an overreach exceeding 20% was observed, and the relay does not trip for a fault 30% beyond the relay reach.

9.14 MODIFIED DECISION LOGIC PROCESS

The relay overreach at high SIR is associated with a burst of up and down counts, which sometimes cause the decision logic counter to reach a trip level on the count of 5. For a fault of SIR of 4.6, it was observed that due to the noise, particularly D(k) differencing noise, the measurand errors at high SIR can cause the decision logic counter to be incremented by steps of 2, for a fault beyond the relay reach, which inevitably causes the reach accuracy to deteriorate. In order to improve the relay reach accuracy, the decision logic process was modified as follows:

1 - A D(k) threshold is set for a fault at the relay reach for SIR of 4.6 and above, such that the inner zone region is disabled, thus permitting single increment of the decision logic counter. This maintains a fast operating time at low SIR and reduces the relay operating time at high SIR. The average measured D(k) magnitude for a fault at the relay reach, for SIR of 4.6 is 740 DCL.

2 - The decision logic counter is decremented by 2 for an out of zone measurement. Thus the relay operating time becomes slower for a fault near the protected zone boundary.

3 - The trip level is increased from 5 to 6 counts.

9.14.1 Relay reach accuracy using the modified decision logic process

The relay reach accuracy for the 128 km line is not affected. For the 24 km line, the relay reach accuracy is shown in Table 9.1:

SIR	Overreach
2.6	5%
4.6	5%
5.8	6%
7.7	10%
11.6	14%
17.6	> 20%

Table 9.1 : Relay overreach for 24 km line

With respect to a fault at SIR 17.6, approximately 30% operation was observed for a fault 20% beyond the relay reach. At this stage, the relay operation must be inhibited for a fault at the relay reach, for SIR of 17.6.

9.14.2 Noise threshold optimization

For a fault at the relay reach, for SIR of 17.6, the average magnitude of D(k) is 12 DCL. In order to ensure that the relay does not operate at this D(k), a D(k) threshold of 14 DCL is set. Thus if D(k) magnitude is smaller than 14 DCL, the measurement is considered unreliable and the decision logic counter is decremented. Fig. 9.19 shows the relay reach accuracy with the 14 DCL D(k) threshold, for a given SIR.

9.14.3 Relay operating time

The relay operating time was tested using the new D(k) threshold and the modified decision logic process (see Section 9.14).

9.14.3.1 128 km Line

The relay operating time for the double end fed 128 km line is not affected (see Section 9.12.1).

9.14.3.2 24 km Line

Fig. 9.20 shows the relay operating time for various SIR, 90 degree inception angle. The effect of disabling the inner zone region for SIR of 4.6 and above do not affect the relay operating time considerably, with only an additional 1 ms observed (see Section 9.12.2). However, the relay operation becomes inconsistent for SIR of 17.6, due to D(k) threshold. A similar relay operating time characteristic is observed for 0 degrees fault inception angle, Fig. 9.21.

9.15 VOLTAGE AND CURRENT THRESHOLD

For the test described above, a D(k) threshold of 14 DCL is set. Conventionally, it is more appropriate to express the thresholds in terms of the relaying voltage and current.

As described in Section 9.14.2, the relay operation must be inhibited for a fault at the relay reach, for SIR 17.8, thus the thresholds are set for the Fourier Transformed relaying voltage and current. With this respect, it must be noted that for a fault at the relay reach, the transformed components have equal magnitude. This permits the use of a similar threshold magnitude for the transformed components. For a fault at the relay reach for SIR of 17.8, the CCD filter input corresponds to 360 DCL, which represents 9% of the nominal signal inputs. Internal to the relay, the transformed components have a magnitude of + and - 800 DCL, thus a positive threshold of $0094 and a negative

threshold of $FF6B are used. In order to reduce the burden of the processor unit, the negative part of the voltage and current components are inverted, thus enabling comparisons to be made against the positive threshold only.

The relay operating time obtained using the relaying voltage and current signals, is similar to that obtained using D(k) threshold (as described in Section 9.14.3).

9.16 SIGNAL PRE-CONDITIONING

The finite transform solution encounters problems due to the exponential offset in the relaying current signals and high frequency components. The effect of the exponential offset in the relaying current signal causes an error in the measured impedance, resulting in considerable relay overreach. The basic scheme described in Chapter 4 is based on the first order approximation utilizing 50 Hz parameters which is not acceptable over the whole range of frequencies [4]. High frequency components caused by travelling waves cannot be avoided and it has therefore been necessary to filter the relaying voltage and currents in such a way as to band limit their frequency content before the algorithm is implemented. Although the fault generated high frequency transients theoretically contain spectral components throughout the whole spectrum, they are nevertheless characterized by travelling wave components between the fault and the relaying point. In practice, it is necessary to suppress the travelling wave components before the algorithm is implemented, particularly for a fault at the relay reach. Swift [28], showed that the estimate of the travelling wave component frequency F_{tw} can be obtained using the formula:

$$F_{tw} = \frac{A\ C_{tw}}{\ell} \qquad \text{--- 9.7}$$

where ℓ is the distance between the fault and the relaying end, C_{tw} is the speed at which the travelling wave propagate and A is a coefficient which may vary between 0.25 and 0.5. Providing the line is less than 200 km, such that the effect of shunt capacitance can be neglected, a 600 Hz travelling wave frequency component is estimated for a fault at 160 km (phase to earth fault at the reach point). For shorter lines, the travelling wave component is of higher frequency, thus the FIR filters must be capable of filtering frequency components of 600 kHz and above. In order to meet the above requirements, consideration was given to the use of pre-conditioning filters employing an 8 stage FIR filter with a transfer function taking the form of Eqn. 9.8:

$$H(z) = (1 + z^{-1} + z^{-2} + z^{-3})(1 - z^{-5}) \qquad \text{--- 9.8}$$

In order to implement the discrete processing solution, it is required to extract the finite Fourier Transform components. In order to provide a fast convergence towards the post fault measurements consideration was given to the use of a short window of 1.25 mS window, for which the transfer function of the filters can be written as:

$$H_1(z) = z^{-1} + 0.809\ z^{-2} + 0.309\ z^{-3} - 0.309\ z^{-4} - 0.809\ z^{-5} \qquad \text{--- 9.9}$$

and

$$H_2(z) = 0.588\ z^{-2} + 0.951\ z^{-3} + 0.951\ z^{-4} + 0.588\ z^{-5} \qquad \text{--- 9.10}$$

where $H_1(z)$ and $H_2(z)$ are the cosine and sine FIR filter transfer functions respectively. The above filtering requirements, the

preconditioning and the extraction of the finite Fourier Transform components, can be achieved using combined FIR filters.

9.16.1 FIR Filter combination

In order to implement the signal preconditioning and the extraction of the finite Fourier Transform components on the existing hardware, consideration was given to combining the FIR filters. Consider two FIR filters responses, $h_{1(n)}$ and $h_{2(n)}$. The duration of $h_{1(n)}$ is N1 samples, $h_{1(n)}$ is nonzero in the interval $0 < n < N1-1$. The duration of $h_{2(n)}$ is N2 samples, $h_{2(n)}$ is nonzero in the interval $0 < n < N2-1$. $h_{1(n)}$ convolves with $h_{2(n)}$ and the combined impulse response $h_{c(n)}$ is nonzero in the interval $0 < n < N1+N2-1$ [29].

$$h_{c(n)} = \sum_{m=0}^{n} h_{1(m)}\ h_{2(n-m)} \qquad \text{--- 9.11}$$

Applying Eqn. 9.11 to Eqns. 9.8 and 9.9 gives the combined cosine transformation filter $H_{cc}(z)$ in the form of Eqn. 9.12:

$$H_{cc}(z) = 0.3416\ z^{-1} + 0.618\ z^{-2} + 0.7236\ z^{-3} + 0.6180\ z^{-4} - 0.6180\ z^{-6} - z^{-7} - z^{-8} - 0.6180\ z^{-9} + 0.2764\ z^{-11} + 0.3820\ z^{-12} + 0.2764\ z^{-13} \qquad \text{--- 9.12}$$

Similarly the combined sine transformation filter transfer function can be written as:

$$H_{cs}(z) = 0.1910\ z^{-2} + 0.500\ z^{-3} + 0.8090\ z^{-4} + z^{-5} - 0.8090\ z^{-6} + 0.309\ z^{-7} - 0.309\ z^{-8} - 0.809\ z^{-9} - z^{-10} - 0.809\ z^{-11} - 0.5\ z^{-12} - 0.910\ z^{-13} \qquad \text{--- 9.13}$$

The impulse responses of the two filters $H_{cc}(z)$ and $H_{cs}(z)$ is shown in Fig. 9.22.

9.16.2 Combined filter frequency responses

Figs. 9.23a and 9.23b shows the frequency responses of the combined filters, $H_{cc}(j\omega)$ and $H_{cs}(j\omega)$; driven at 2.7 kHz sampling rate, and the Butterworth analogue low-pass filters. The infinite attenuation occurring at zero frequency is well appreciated, since it is virtually eliminating the exponential offset, which is required for the algorithm implementation as described in Section 9.9.2. The second zero in the frequency response occurs at 600 Hz, which corresponds to 30 dB and 21 dB attenuation by the cosine and sine combined filters respectively. The third zero occurs at 900 Hz which corresponds to over 40 dB attenuation. The significance of having the second at approximately 0.2 of the sampling rate is the capability of the filter to reject the travelling wave component for a fault at 160 km from the relaying end (phase to earth fault), since 160 km is the maximum line length for the algorithm implementation. In practice, the sampling rate can be adjusted so that the filters have a zero at the frequency at which the travelling wave component occurs for a fault at the relay reach, since the accuracy is most needed for a fault at the relay reach.

9.17 COMBINED FILTER IMPLEMENTATION

In order to test the relay performance, using the combined filters, practical difficulties were encountered in accurate setting of the filter impulse responses. As described in Section 9.2, there is a possibility of a small error between similar impulse responses, which can be eliminated by finely adjusting the impulse response of one filter to match its equivalent, using a steady state input. Although it was possible to set the filter impulse responses individually, the fine tuning of the impulse responses can cause an error in the infinite

attenuation at 0 Hz. Alternatively, the relay performance can be studied using the process simulation [4, 18, 19]. The flow chart of the algorithm simulation is shown in Fig. 9.24. The relay performance was studied for both 128 km and 24 km lines, with particular reference to a fault at the relay reach for a given SIR.

9.17.1 0 Degrees fault inception angle relay performance

As described in Section 9.10.2, the relay accuracy is affected by the relaying current exponential component. In order to maintain an accurate relay reach, the exponential component must be eliminated. Fig. 9.25a shows the voltage and current signals, 0 degree inception angle for SIR of 4.6, for a fault at the relay reach, 24 km line. The effect of having infinite attenuation at 0 Hz can be clearly shown in Fig. 9.25b, where the current exponential offset is virtually eliminated. Figs. 9.26a and 9.26b show the fully offset relaying current and the preconditioning filter output on a magnified scale, respectively. The effect of eliminating the exponential offset can be shown in Fig. 9.27a, where D(k) sinusoidal component is virtually eliminated, thus producing a stable X(k) and R(k) measurement. The relay maintains the smooth performance for up to SIR of 23, as shown in Figs. 9.28a and 9.28b.

9.17.2 90 Degrees fault inception angle performance

For most faults within the protected zone, the measured reactance converge to the post-fault value rapidly and one cycle fault clearance can be achieved. However, for faults at the relay reach the filter performance is characterized by a long downward droop in the phase voltage, in the immediate post fault period. Fig. 9.29b shows the output of the preconditioning filter for a fault at the relay reach,

for SIR of 4.6. The phase voltage transient affects the behaviour of the measured reactance in the immediate post fault period in two ways (specified as transient regions). Firstly, the measurements display a transient behaviour for approximately 6 ms (region A in Fig. 6.30b), which is not of great significance. Secondly, the measured reactance converge to region B in Fig. 9.30b, at which the reactance magnitude is approximately 1/3 of that at the relay reach, for approximately 3 ms. For a higher SIR, the phase voltage droop magnitude becomes greater and for a fault at SIR of 23, Fig. 9.31b, where its magnitude is 30% bigger compared with that of SIR of 4.6. Fig. 9.32b shows the behaviour of the measured reactance for a fault at the relay reach for SIR of 23. With respect to a fault at the relay reach for SIR of higher than 4.6, the post fault transient (region B) observed to be of shorter period, when compared with that of SIR of 4.6 and the decision logic counter is capable of preventing an overreach.

9.17.3 Preconditioning filter assessment

The relay performance for 0 degree inception angle shows a smooth performance, since the exponential offset is eliminated. For 90 degree inception angle, the measured reactance shows a rapid convergence toward the post fault values and u.h.s. performance can be achieved. However, for faults at the relay reach, 90 degree inception angle, for a short line, the measured reactance shows a severe transient in the immediate post fault period. With respect to a fault at SIR 4.6 and above, the measured reactance converges to a magnitude smaller than that at the reach point. With reference to Fig. 9.30b, region B, the measured reactance converges to a magnitude smaller than that at the relay reach for approximately 3 ms, which represent 10 to 12 counts for

4 kHz sampling rate. Thus the trip level of the decision logic counter must be greater than 12 counts for faults at the relay reach. Nevertheless, the relay reach integrity and a u.h.s. operation can be maintained if an appropriate decision logic process is used (see Section 10.3.3).

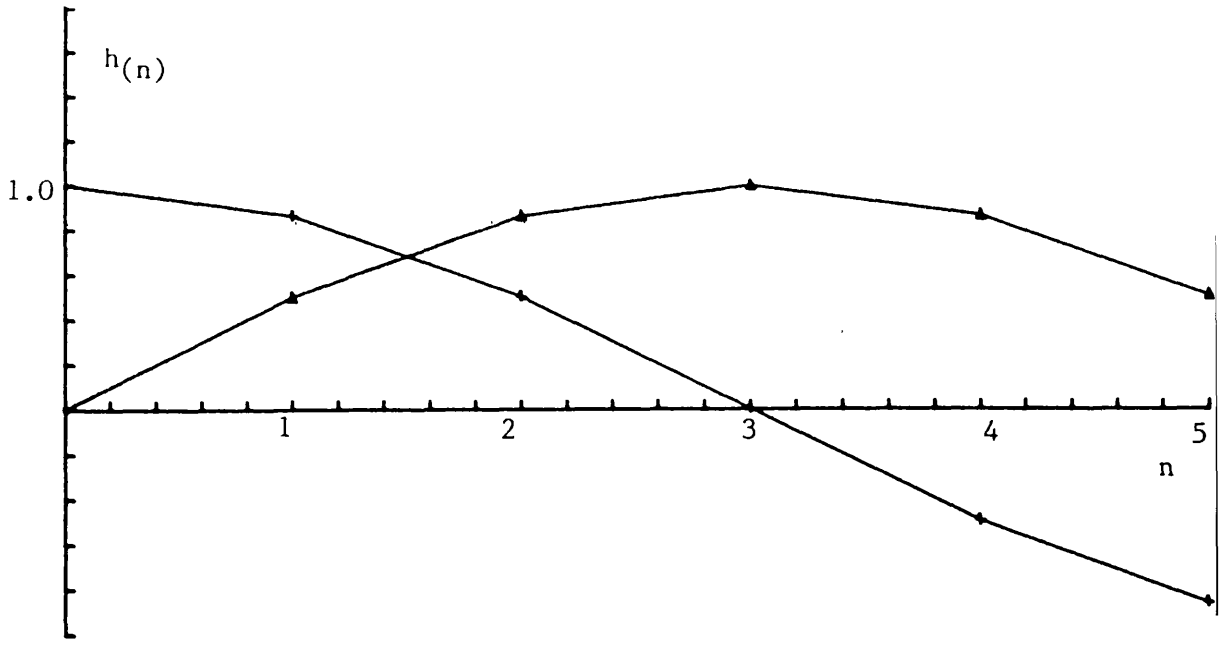


Fig. 9.1 : Sine and cosine convolution filter impulse responses

cosine convolution filter

sine convolution filter

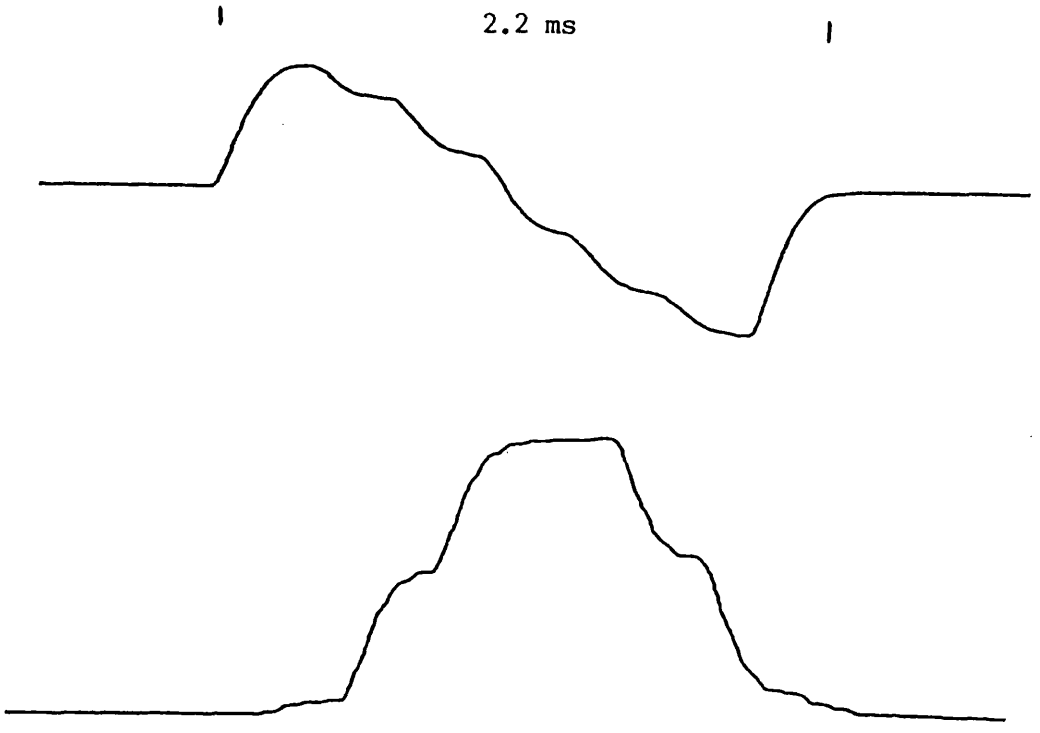


Fig. 9.2 : CCD filter impulse responses

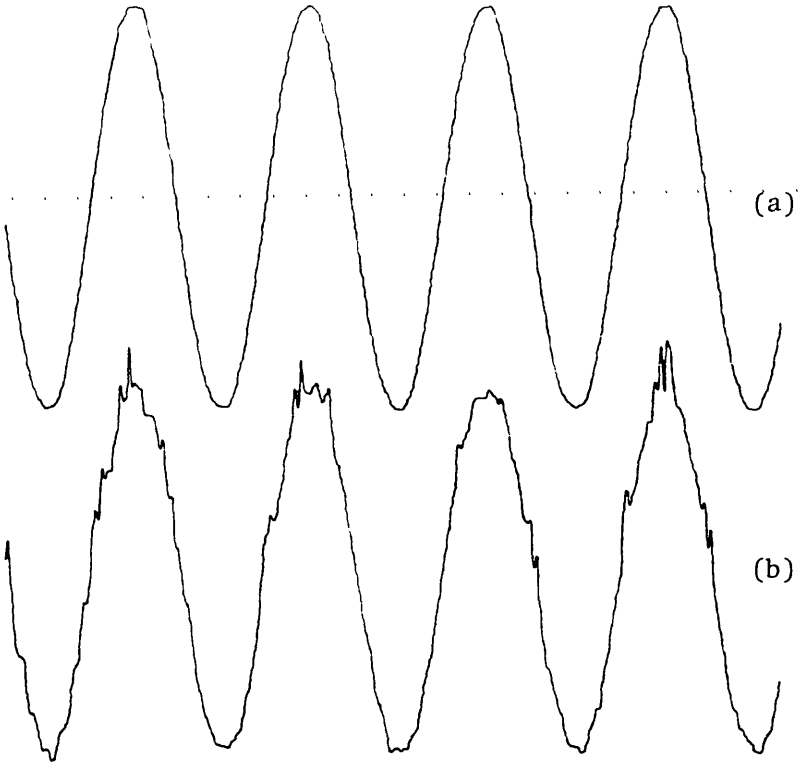


Fig. 9.3 : The 2 ms window cosine convolution filter outputs

(a) - with separate power supply, with the CCD input gate protection diodes removed

(b) - with relay power supply, with the CCD input gate protection diodes removed

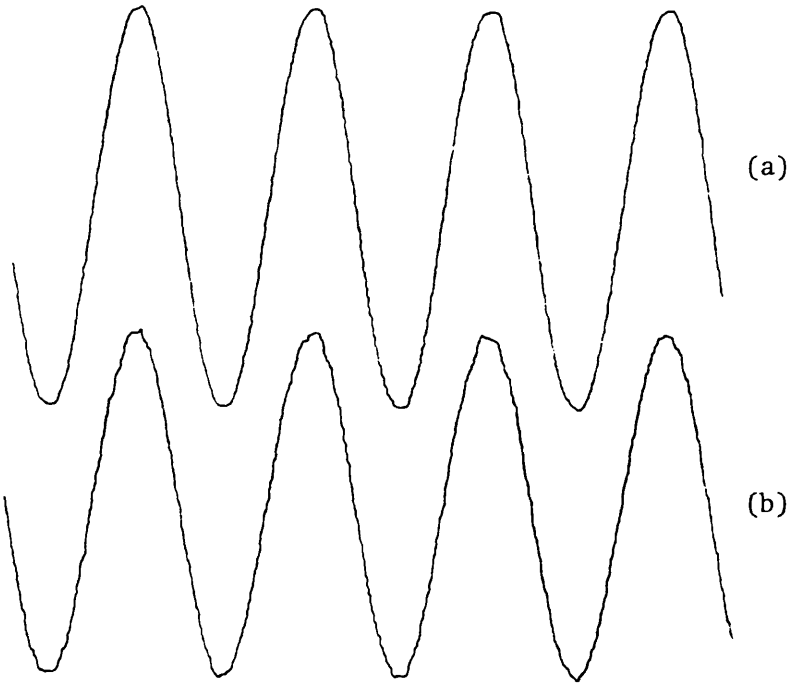


Fig. 9.4 : Effect of the CCD filter input gate protection diodes

(a) - without protection diodes

(b) - with protection diodes

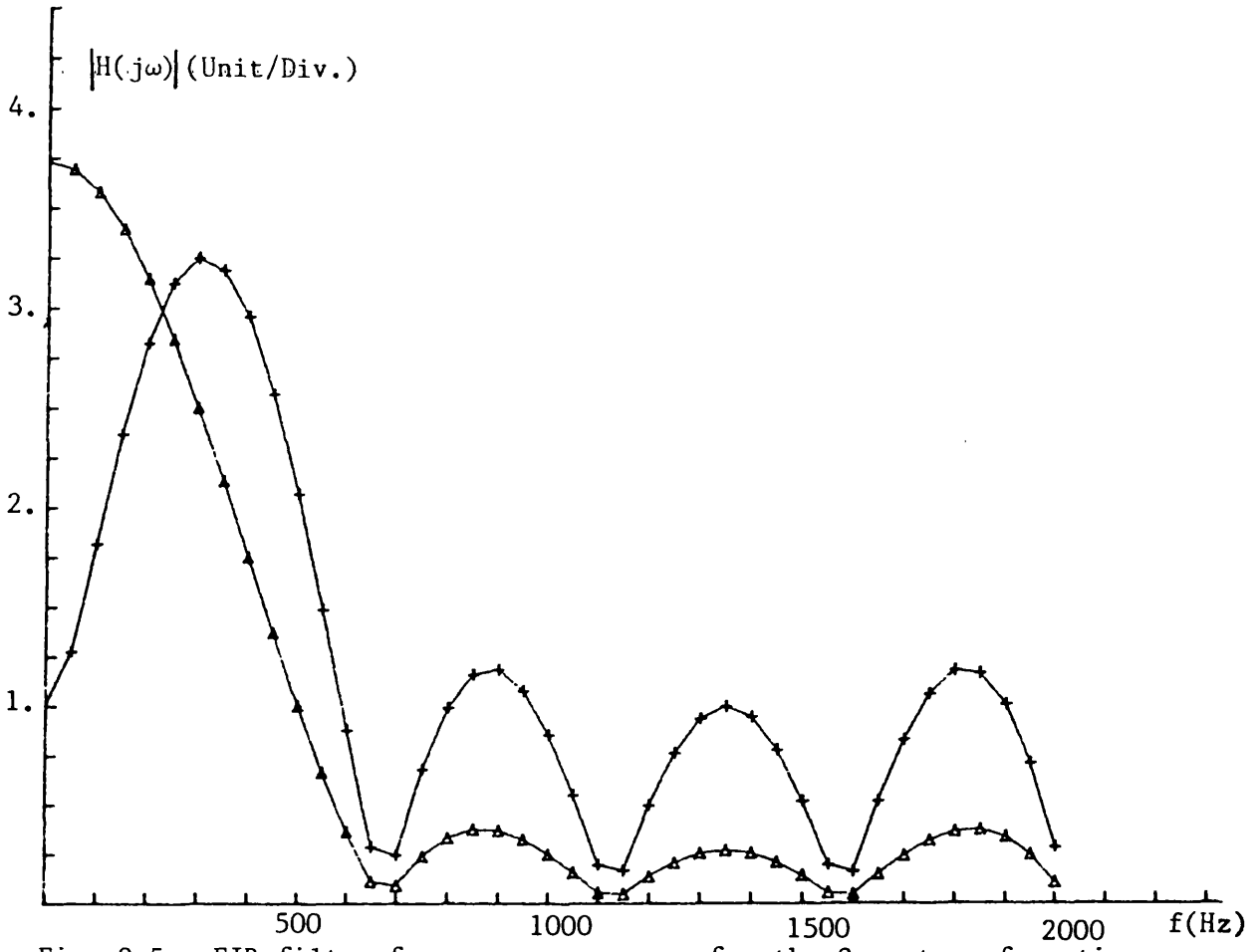


Fig. 9.5 : FIR filter frequency responses for the 2 ms transformation window at 2.7 kHz sampling rate

cosine convolution filter

sine convolution filter

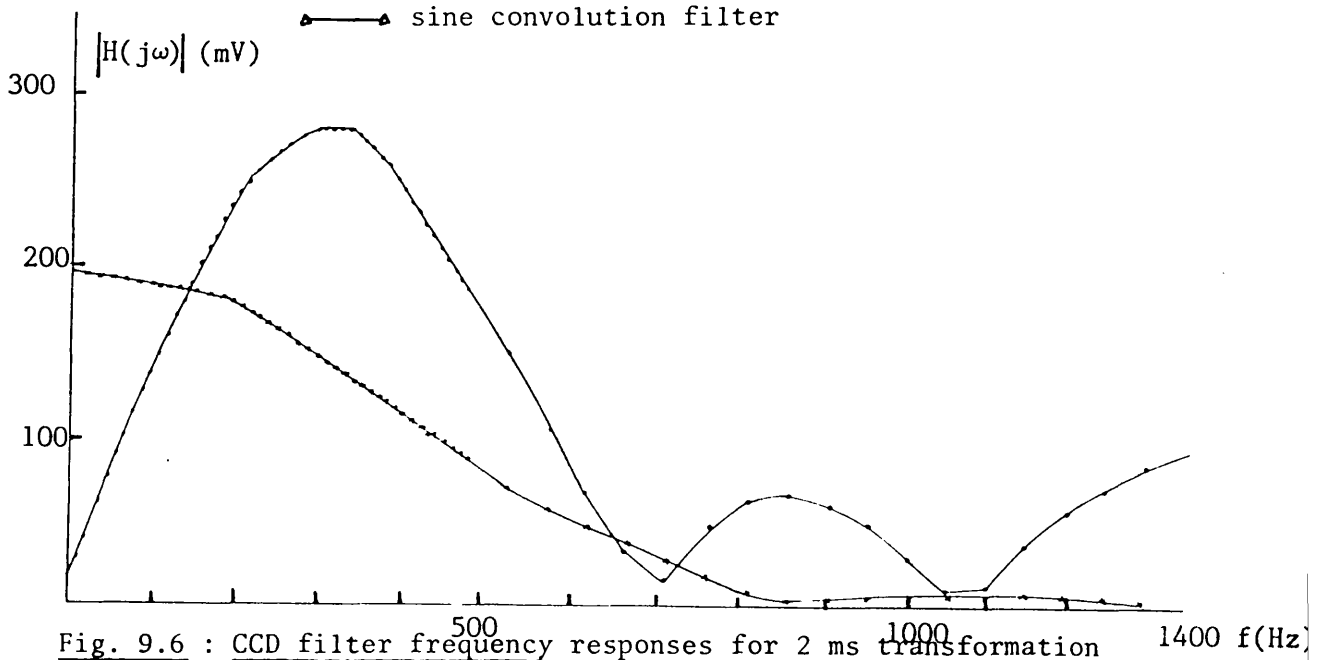


Fig. 9.6 : CCD filter frequency responses for 2 ms transformation window at 2.7 kHz sampling rate

cosine convolution filter

sine convolution filter

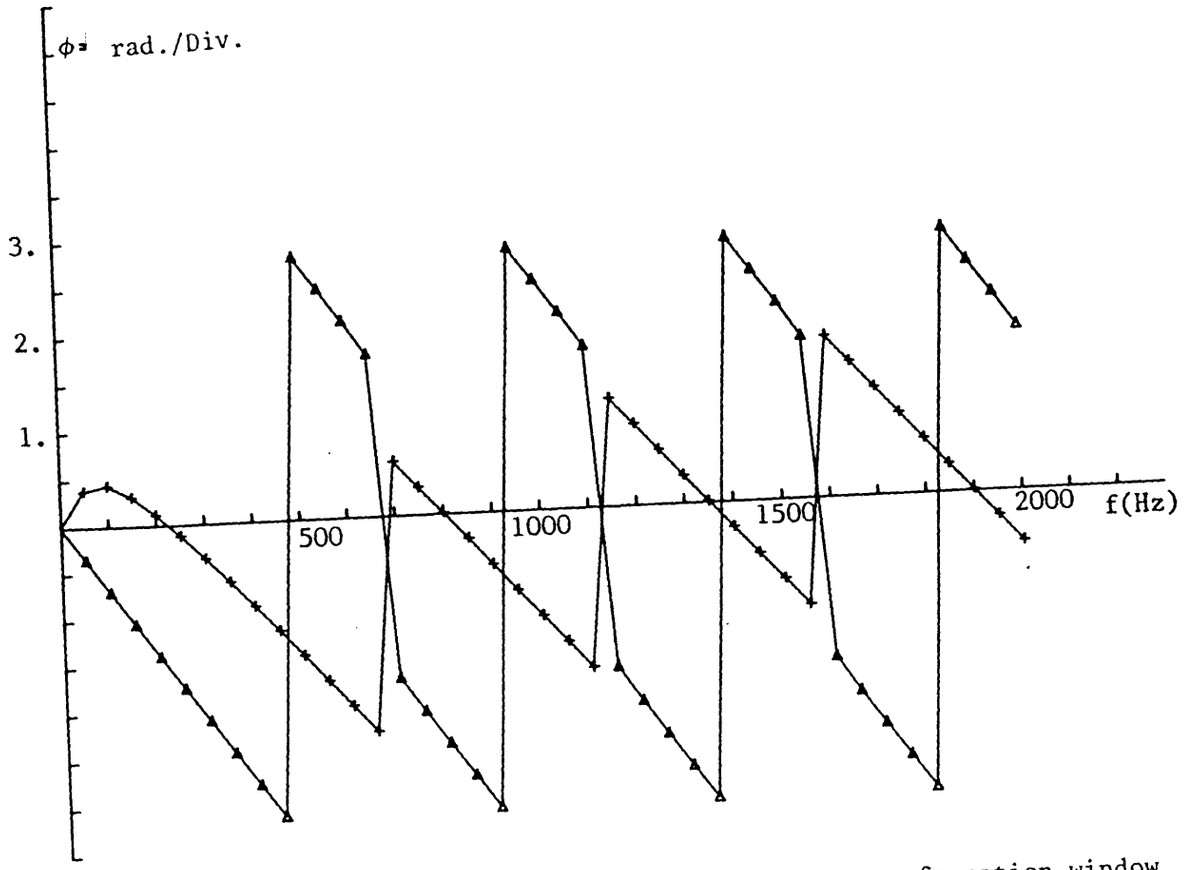


Fig. 9.7 : FIR filter phase responses for the 2 ms transformation window

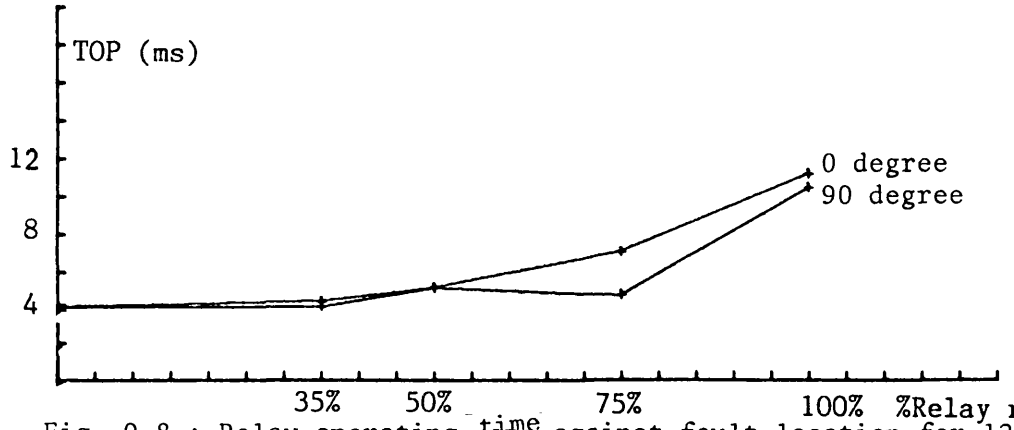


Fig. 9.8 : Relay operating time against fault location for 128 km line, 5 GVA source capacity at the relaying end and 35 GVA at the remote end

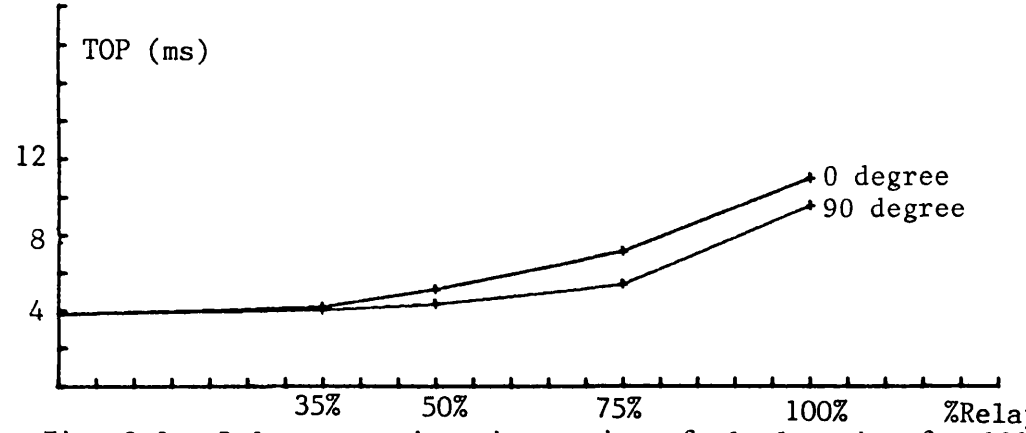


Fig. 9.9 : Relay operating time against fault location for 128 km line, 35 GVA source capacity at the relaying end and 5 GVA source capacity at the remote end

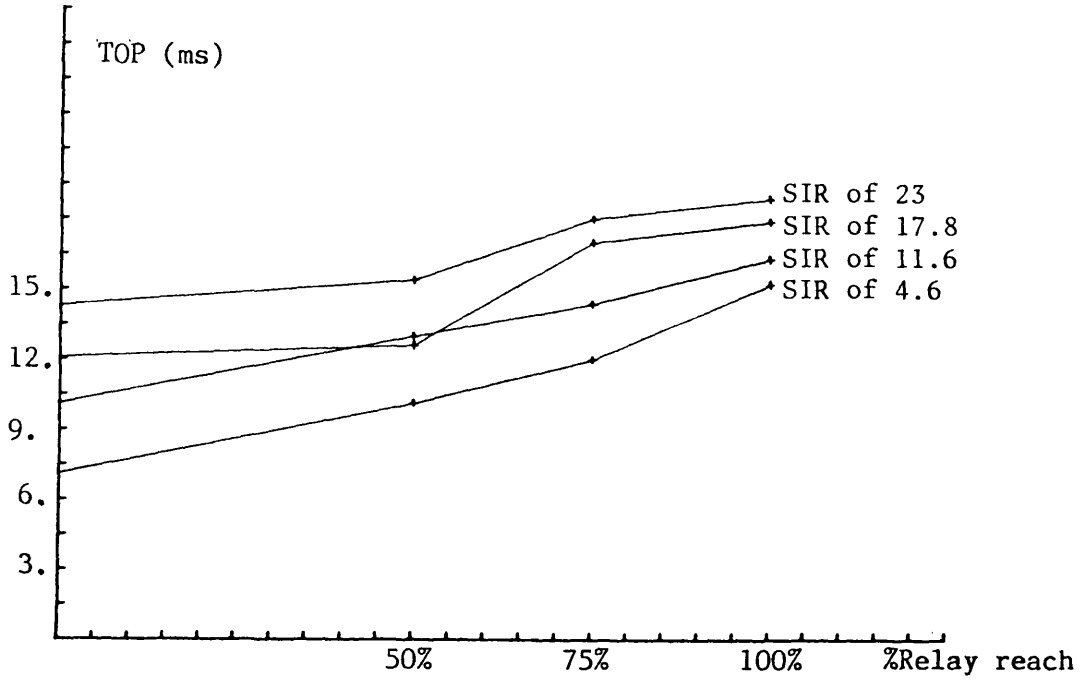


Fig. 9.10 : Relay operating time against fault location for a given SIR. 24 km line, 90 degree fault inception angle

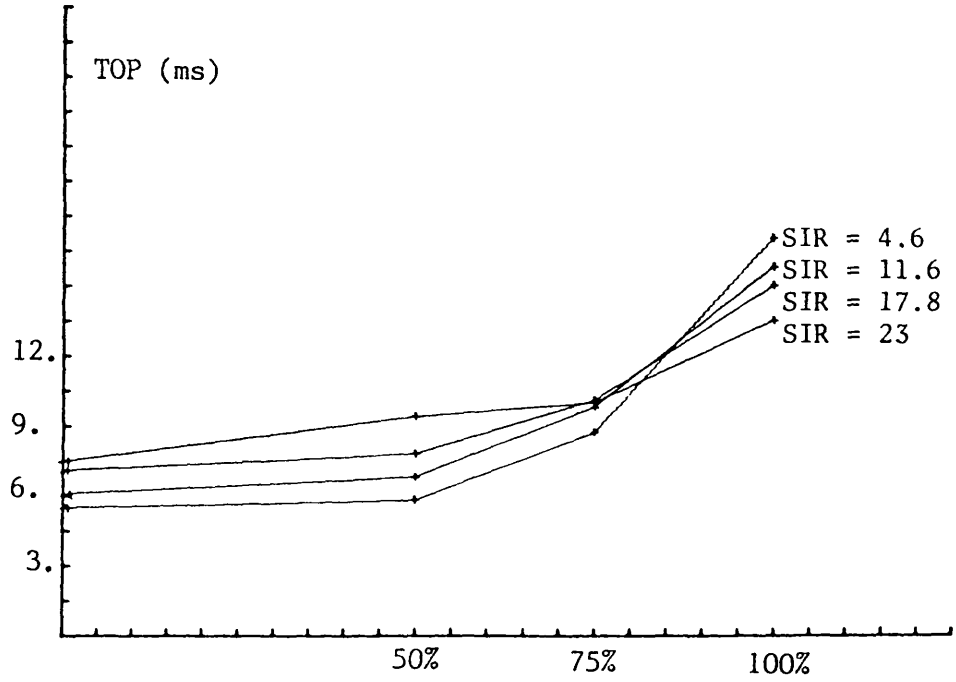


Fig. 9.11 : Relay operating time against fault location for a given SIR. 24 km line, 0 degree fault inception angle

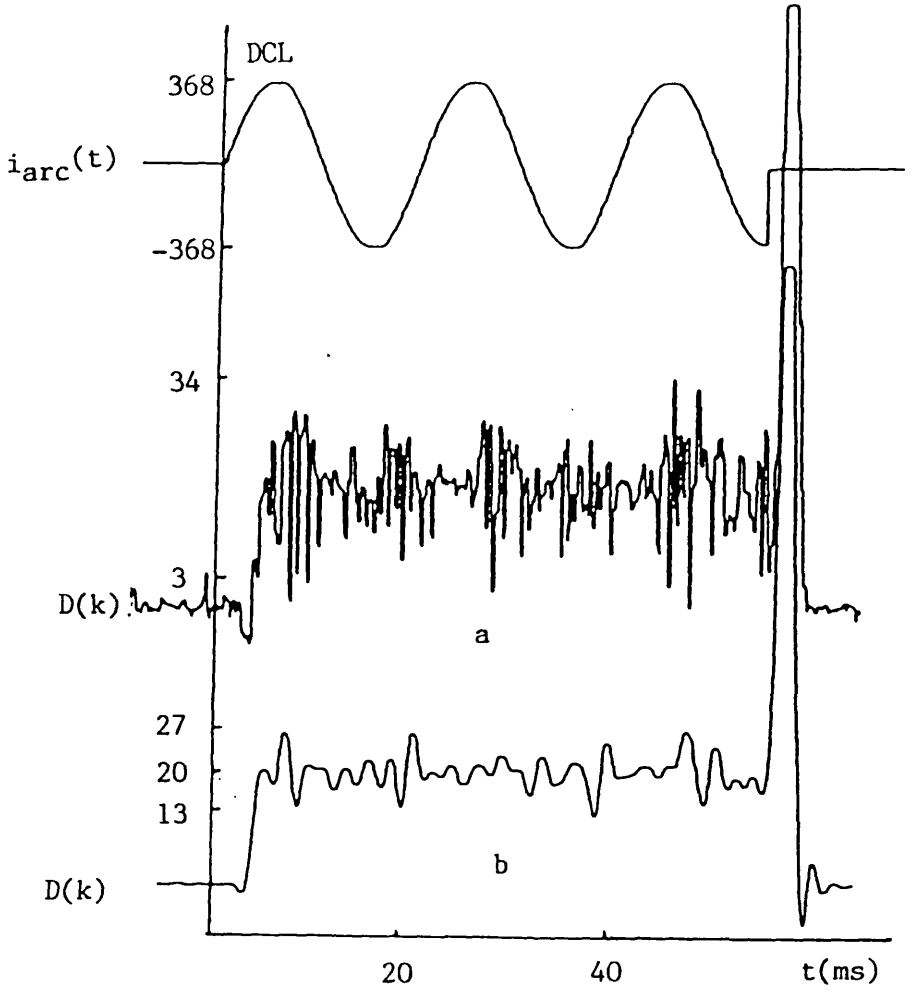


Fig. 9.12: The relaying term D(k) for a fault at 19.2 km (100% relay reach), for SIR of 4.6, 90 degree fault inception angle

a- The D(k) noise due to differencing.

b- Externally filtered D(k), using a second order butterworth filter with cut-off frequency of 500 Hz.

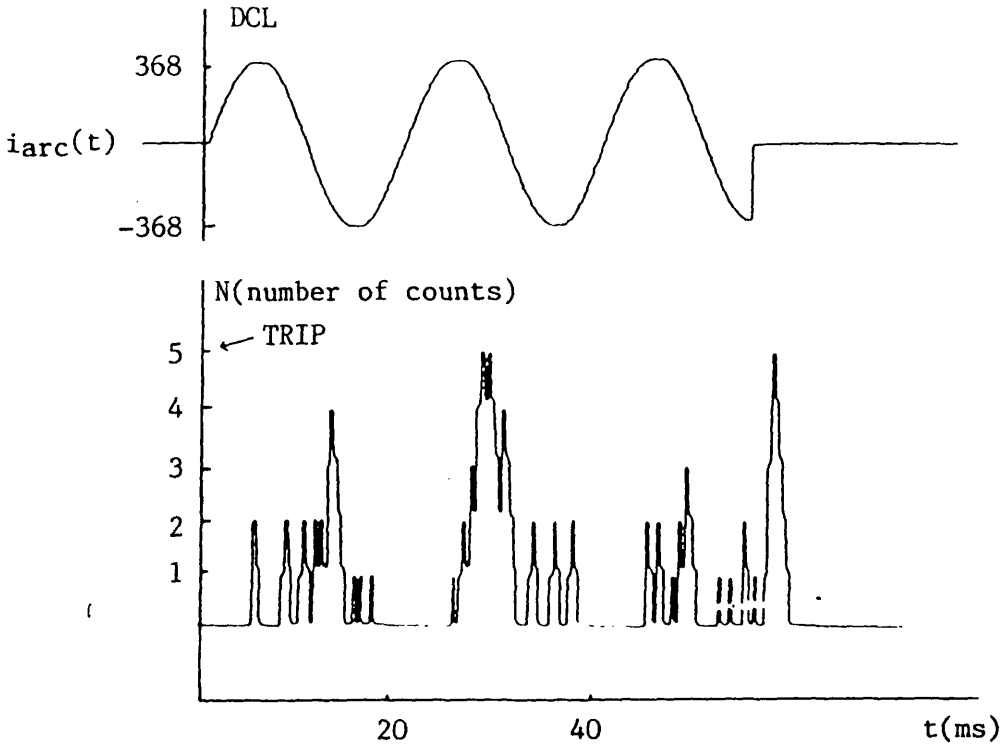


Fig. 9.13: The response of the decision logic for a fault 10% beyond the relay reach, 90 degree inception angle and SIR of 4.6.

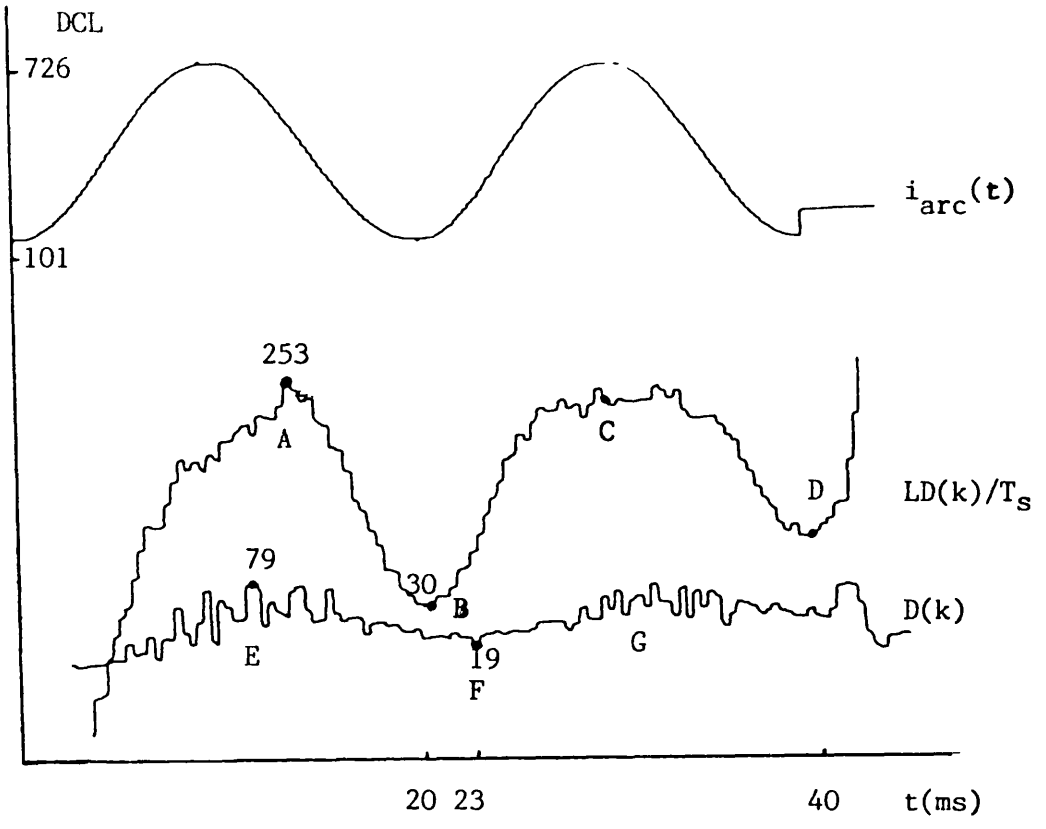


Fig.9.14: The sinusoidal components introduced by the relaying current exponential offset for a fault at 102 km (128 km line). 5 GVA source capacity at the relaying end and 0 degree inception angle.

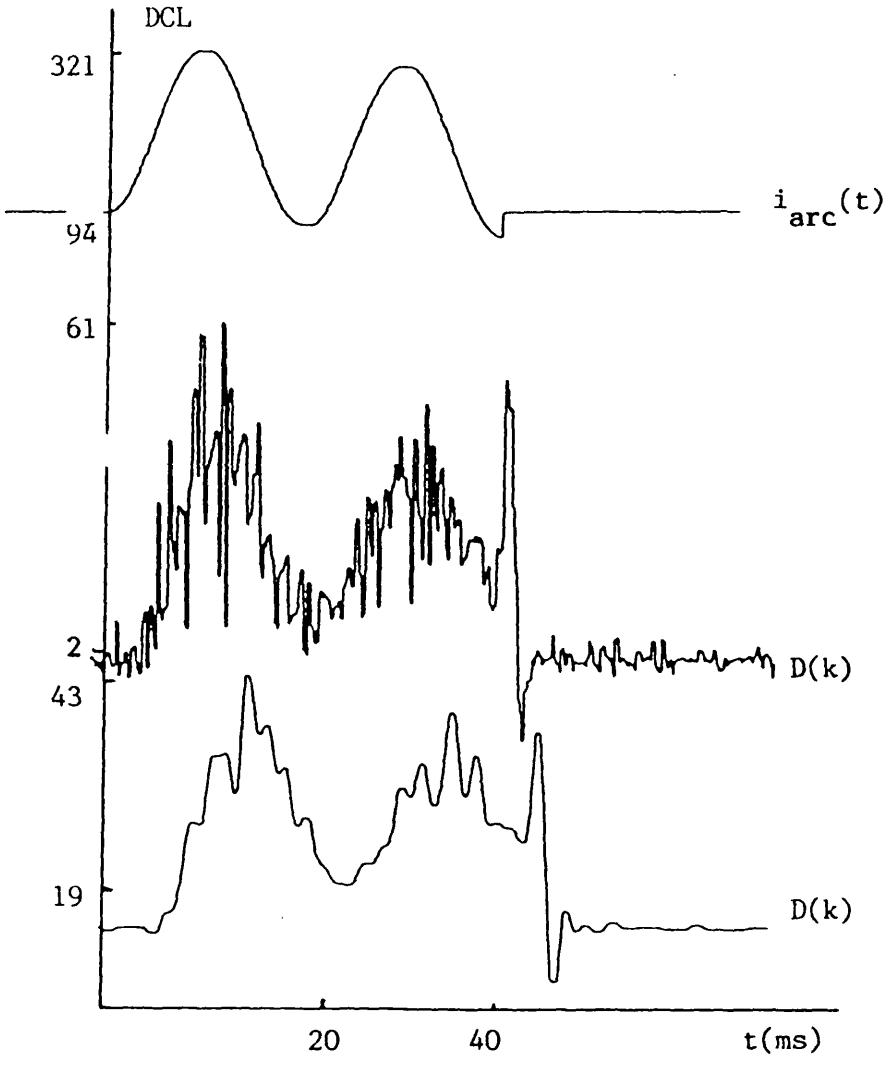


Fig. 9.15a: The behaviour of the relaying term D(k) in the event of the current exponential offset for a fault at 19.2 km (24 km line), 0 degree inception angle and SIR of 4.6.

a- The D(k) sinusoidal component

b- Externally filtered D(k)

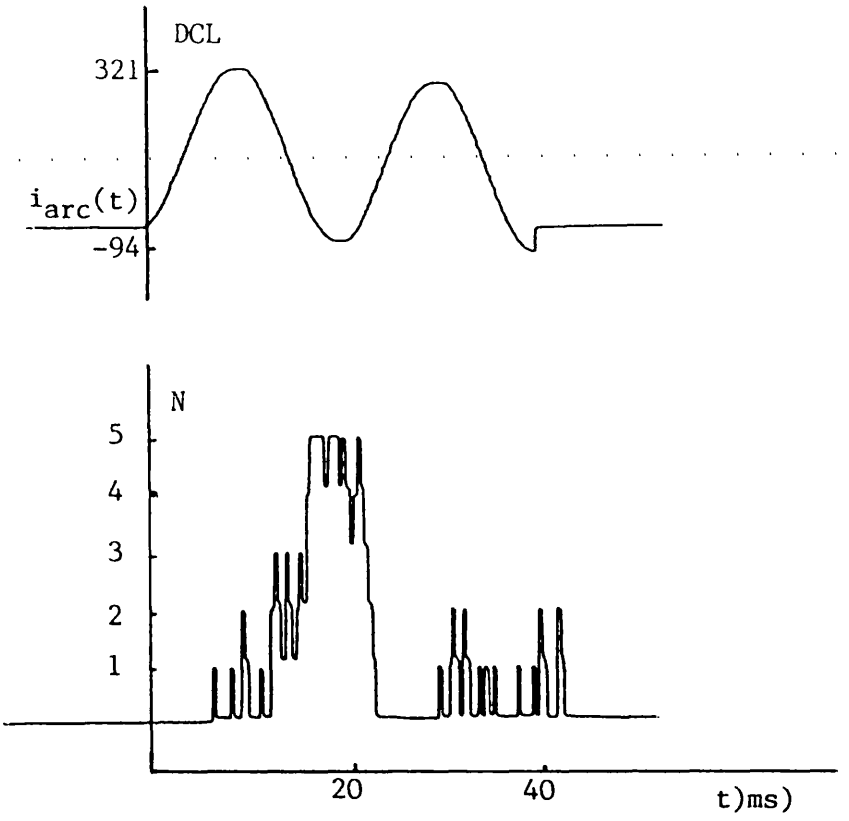


Fig. 9.15b : The response of the decision logic counter for a fault at 10% beyond the relay reach (24 km line). 0 degree inception angle for SIR of 4.6

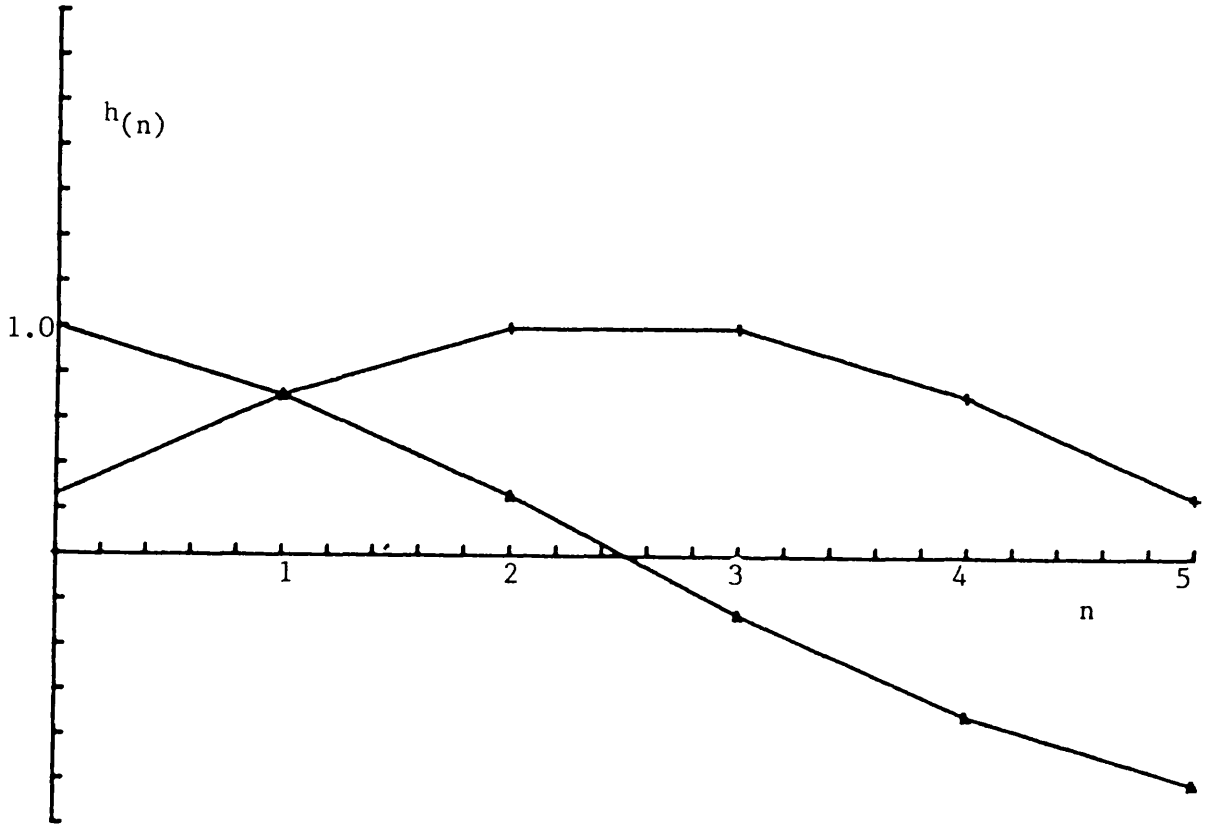


Fig. 9.16a : Phase modified finite Fourier Transform filter impulse responses

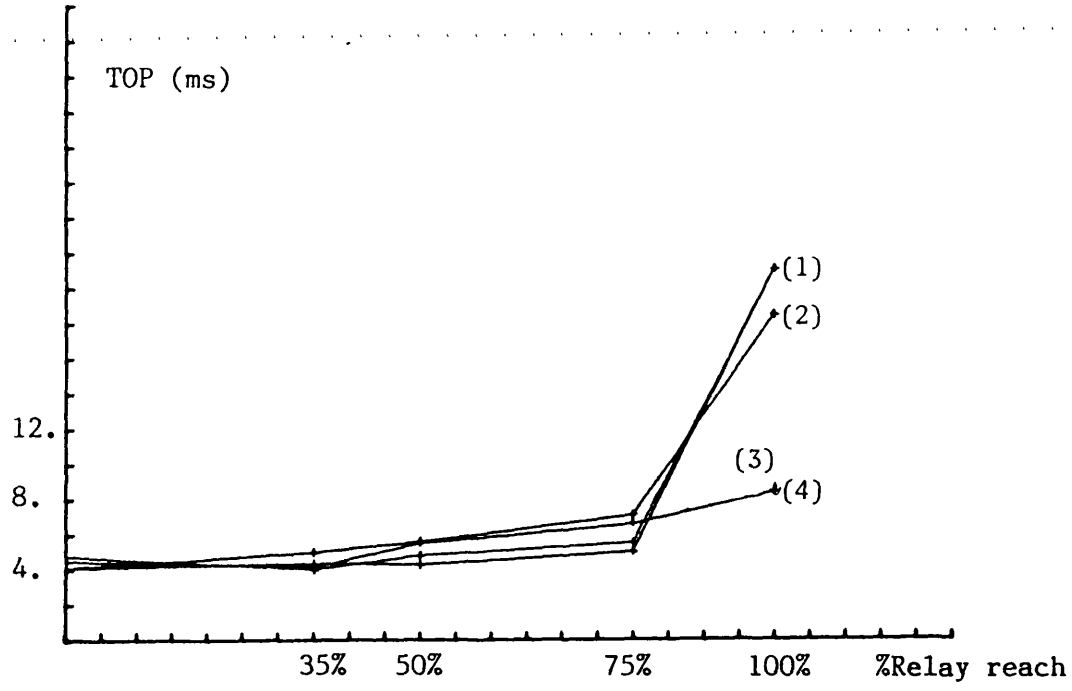


Fig. 9.16b : Relay operating time against fault location (128 km line)

(1) 5 GVA source capacity at the relaying end and 35 GVA souuce capacity at the remote end, 90 degree inception angle
(2) 5 GVA source capacity at the relaying end and 35 GVA source capacity at the remote end, 0 degree inception angle
(3) 35 GVA source capacity at the relaying end and 5 GVA source capacity at the remote end, 90 degree inception angle
(4) 35 GVA source capacity at the relaying end and 5 GVA source capacity at the remote end, 0 degree inception angle

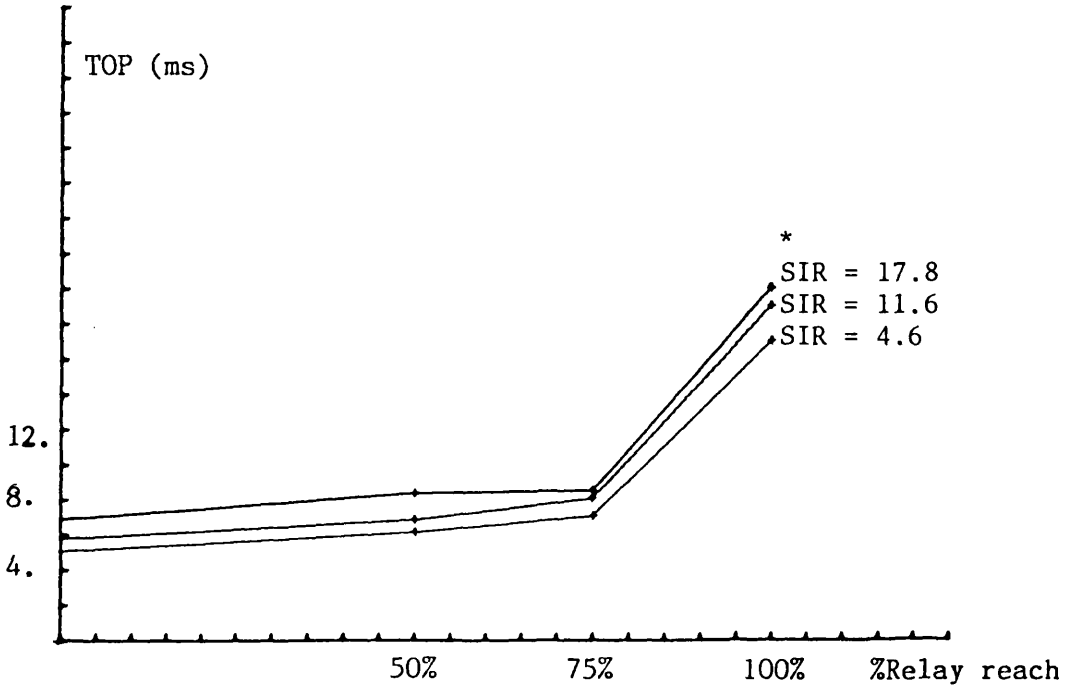


Fig. 9.17 : Relay operating time against fault location for various SIR (24 km line), 90 degree inception angle

* inconsistent operating time is observed at SIR of 23.

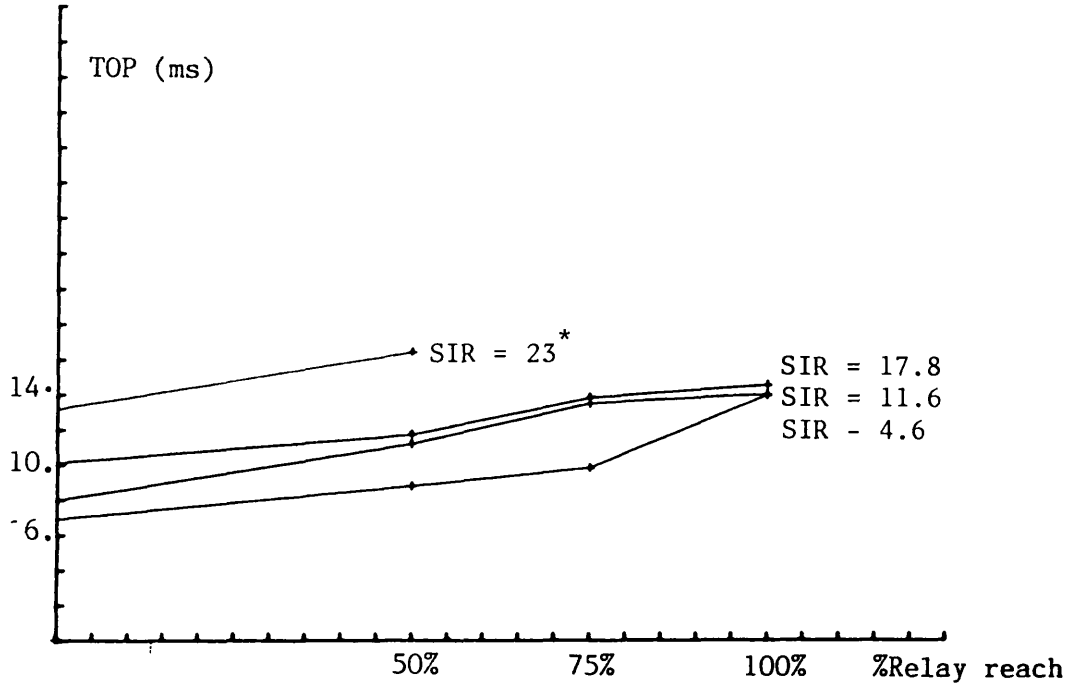


Fig. 9.18 : Relay operating time against fault location for various SIR (24 km line), 0 degree inception angle

*inconsistent operating time is observed for fault at 50% of the relay reach, SIR of 23.

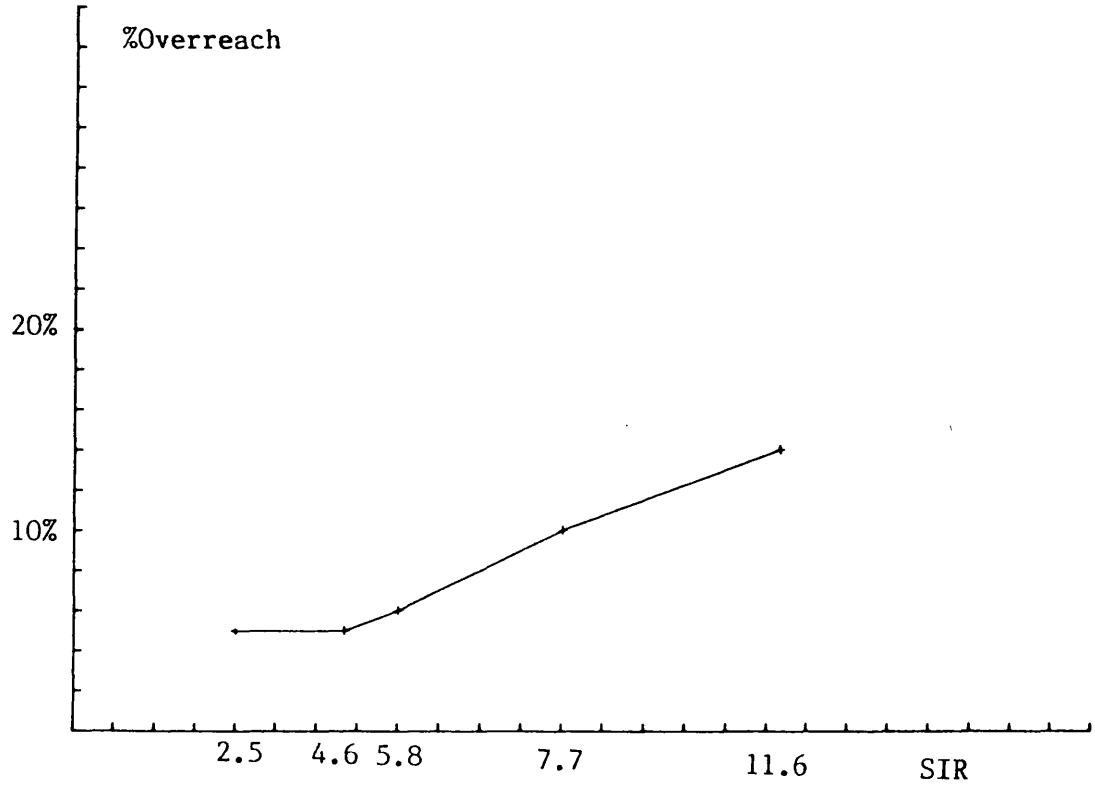


Fig. 9.19 : Relay overreach for a given SIR, D(k) level threshold of 14 DCL, 90 degree inception angle

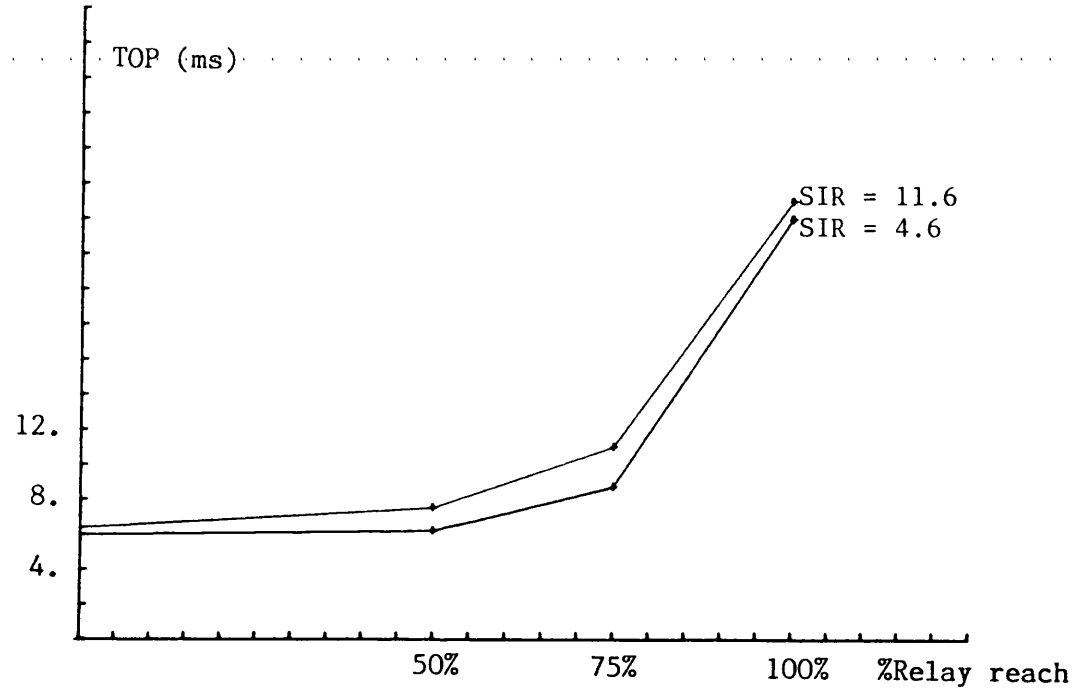


Fig. 9.20 : Relay operating time for 24 km, using the modified decision logic process, 90 degree fault inception angle at a given SIR

*Inconsistent relay operating time for faults at SIR of 18.

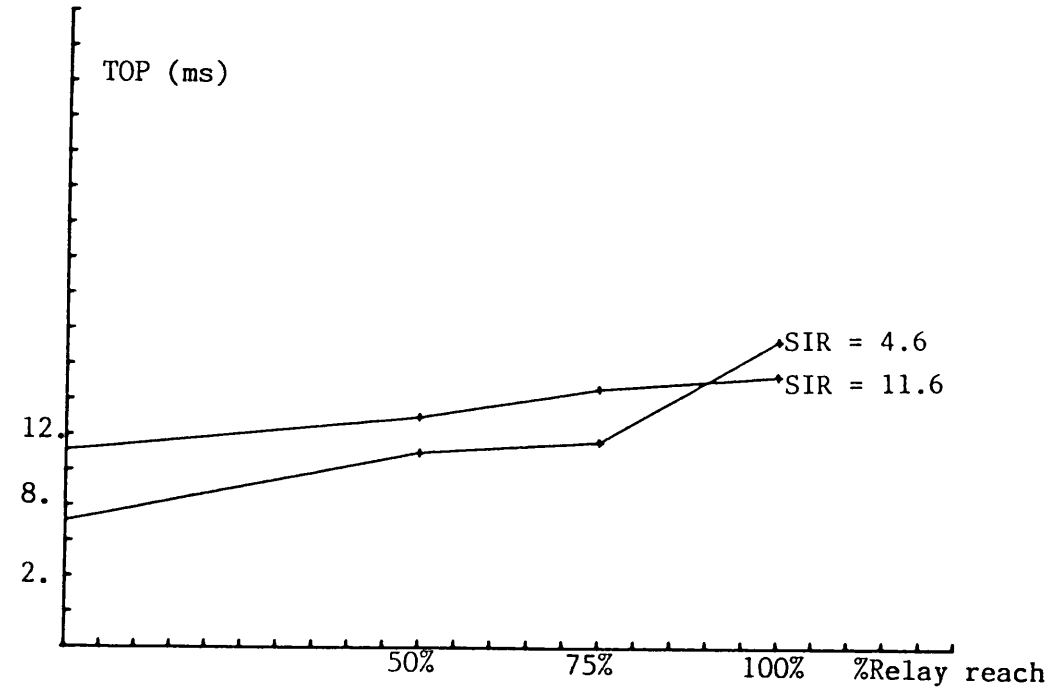


Fig. 9.21 : Relay operating time for 24 km line, using the modified decision logic process, 0 degree fault inception angle for various SIR

*Inconsistent relay operating time for faults at SIR of 18.

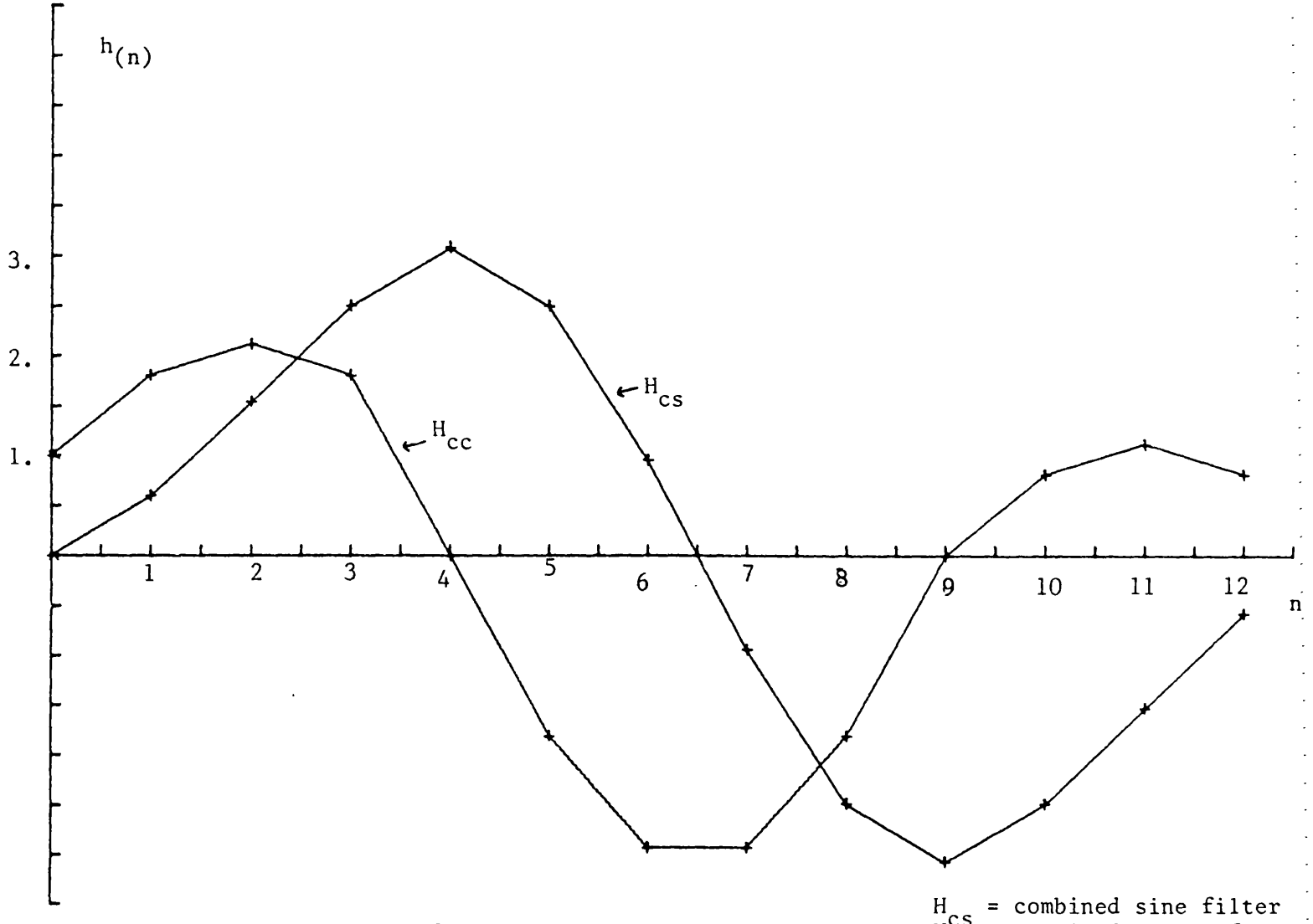


Fig. 9.22 : The combined FIR filter impulse responses

H_{cs} = combined sine filter
H_{cc} = combined cosine filter

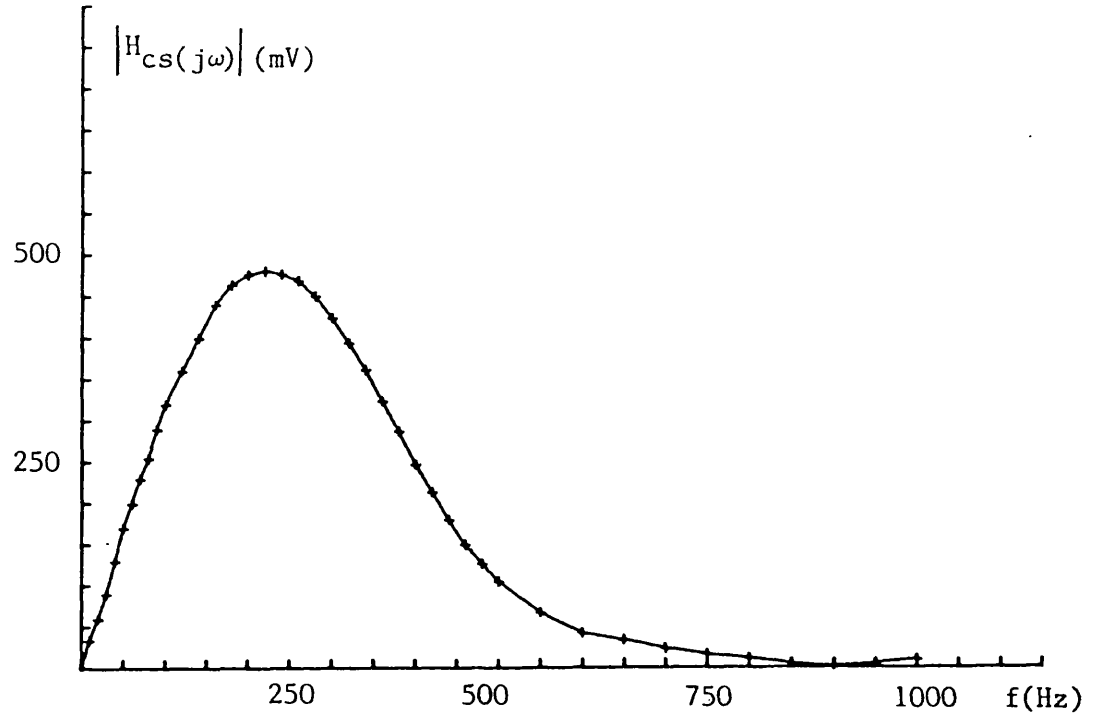


Fig. 9.23a : CCD combined sine filter frequency response for 2.7 kHz sampling rate

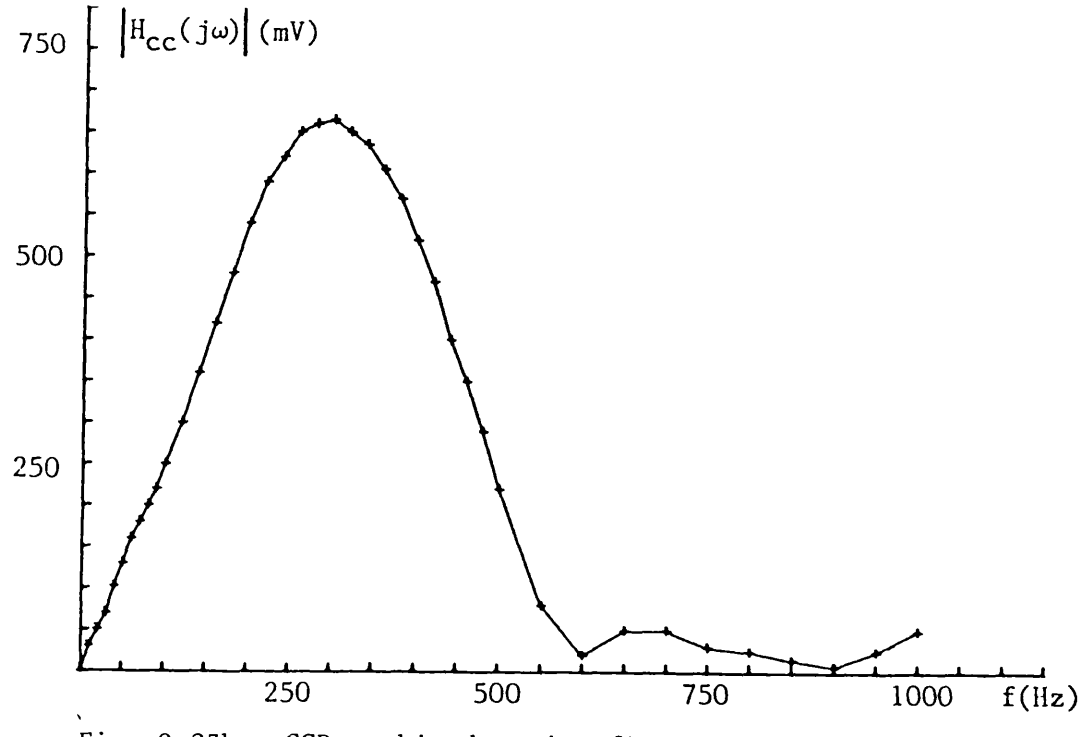


Fig. 9.23b : CCD combined cosine filter frequency response for 2.7 kHz sampling rate

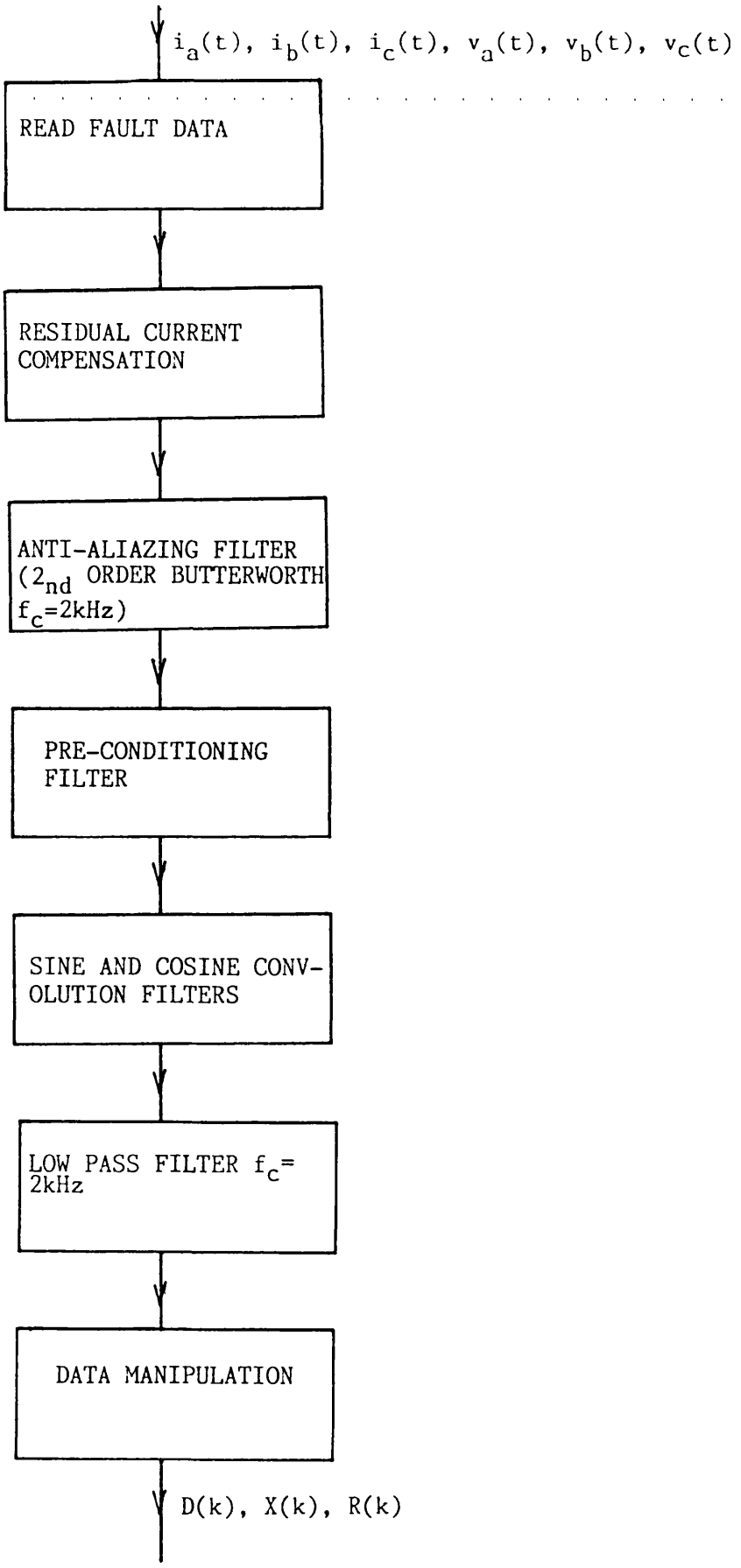


Fig. 9.24 : Algorithm simulation flow chart

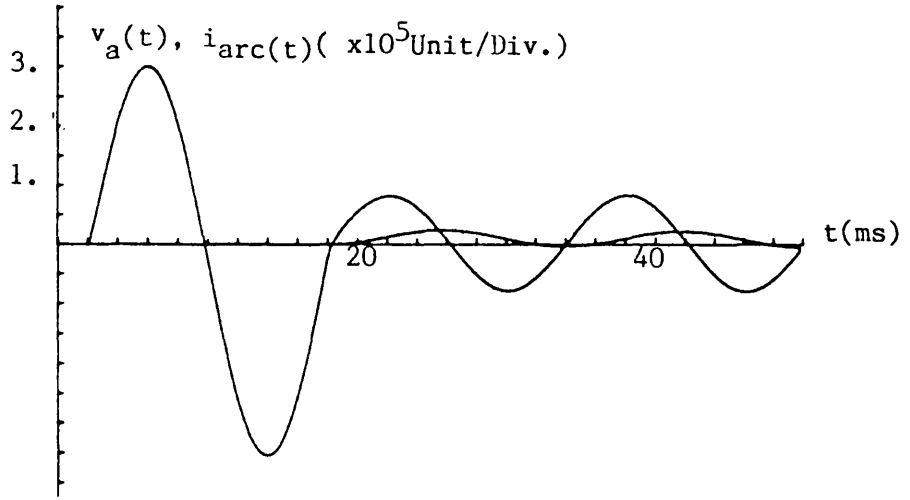


Fig. 9.25a : Primary voltage and current signals for a fault at 19.2 km (24 km line), 0 degree inception angle and SIR of 4.6

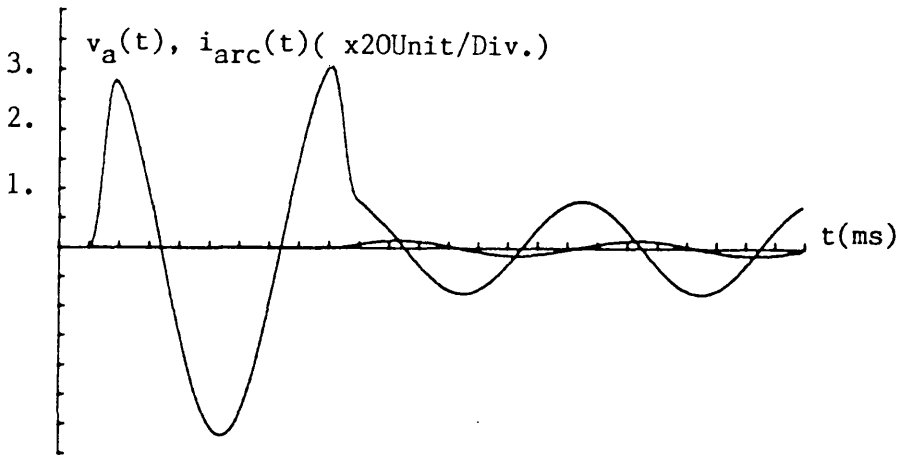


Fig. 9.25b : The primary current for the fault condition of Fig. 9.25a

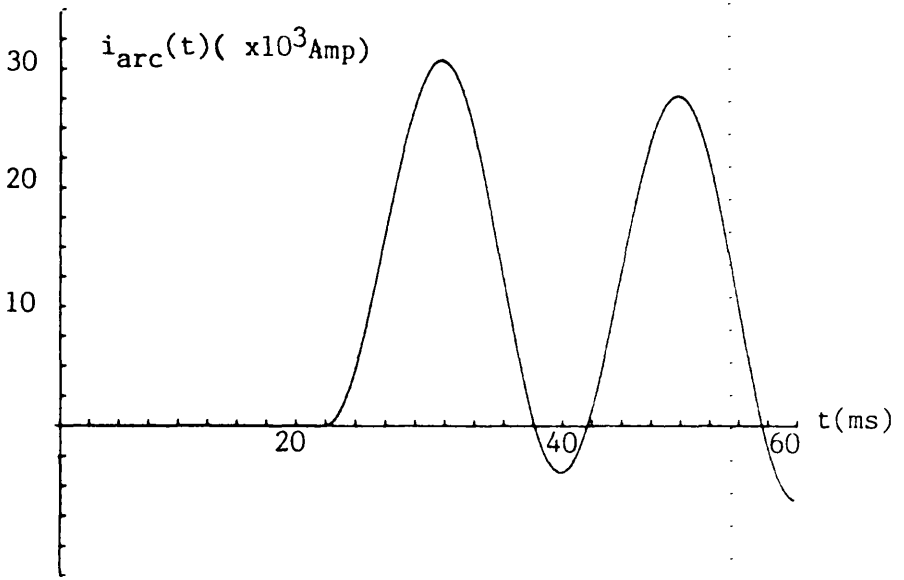


Fig. 9.26a : The input of the pre-conditioning filter for the fault condition in Fig. 9.25a

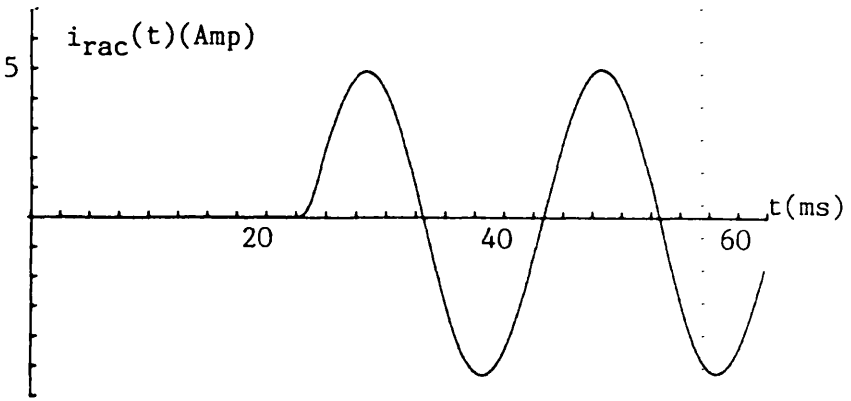
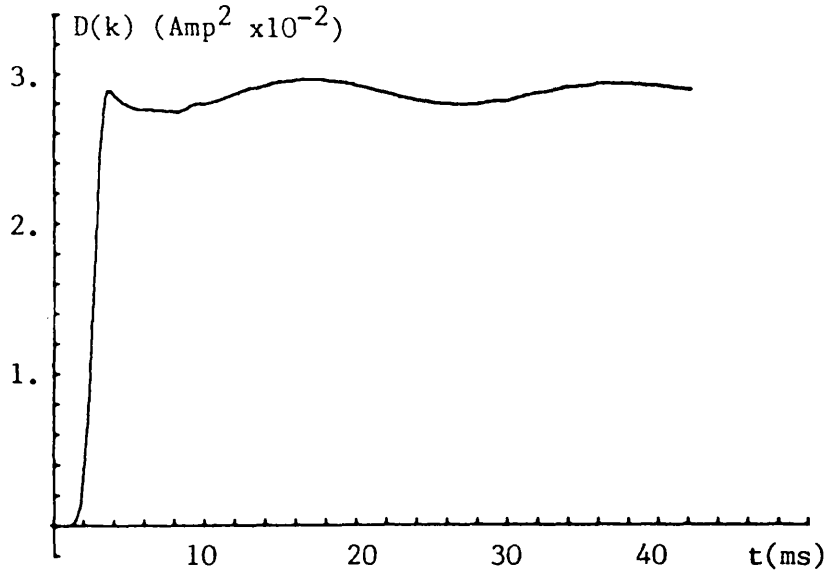


Fig. 9.26b : The output current of the pre-conditioning filter



Fig, 9.27a: The behaviour of D(k) for a fault at the relay reach for 24 km line, 0 degree inception angle and SIR of 4.6.

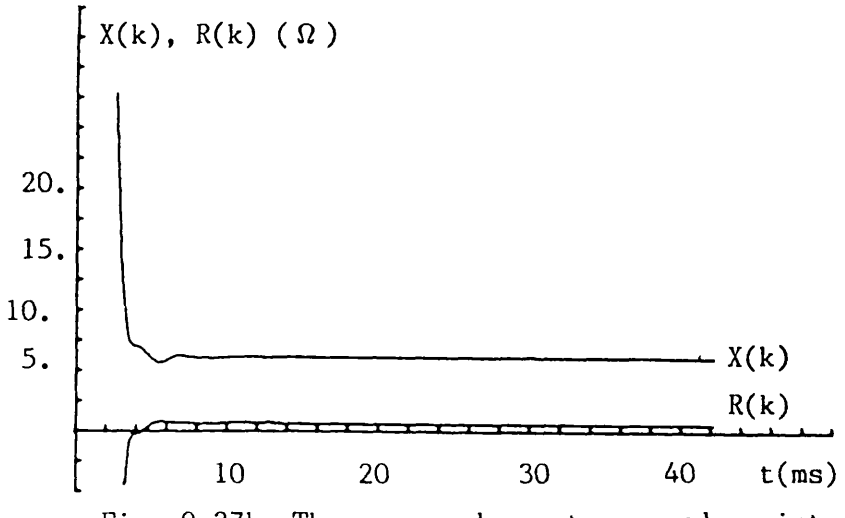


Fig. 9.27b: The measured reactance and resistance for a fault at the relay reach (24 km line), 0 degree inception angle and SIR of 4.6.

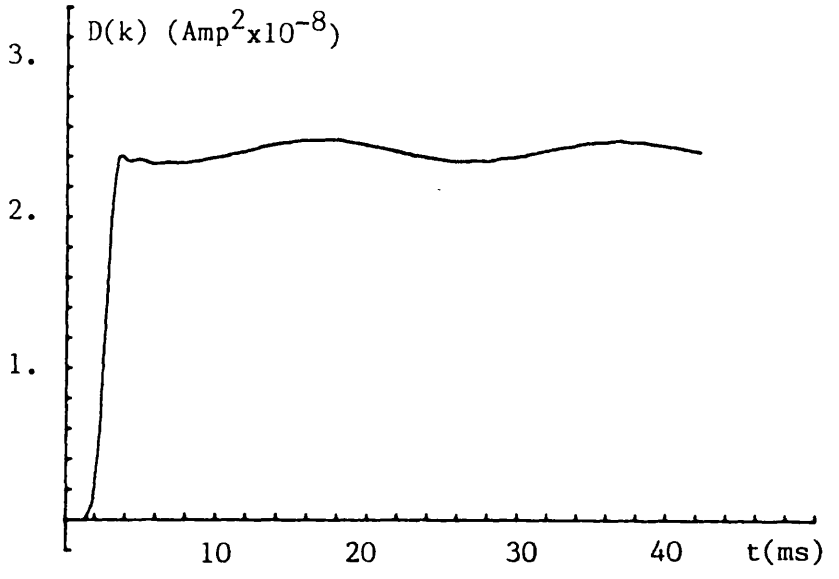


Fig. 9.28a: The behaviour of D(k) for a fault at the relay reach (24 km line) and SIR of 23, 0 degree inception angle.

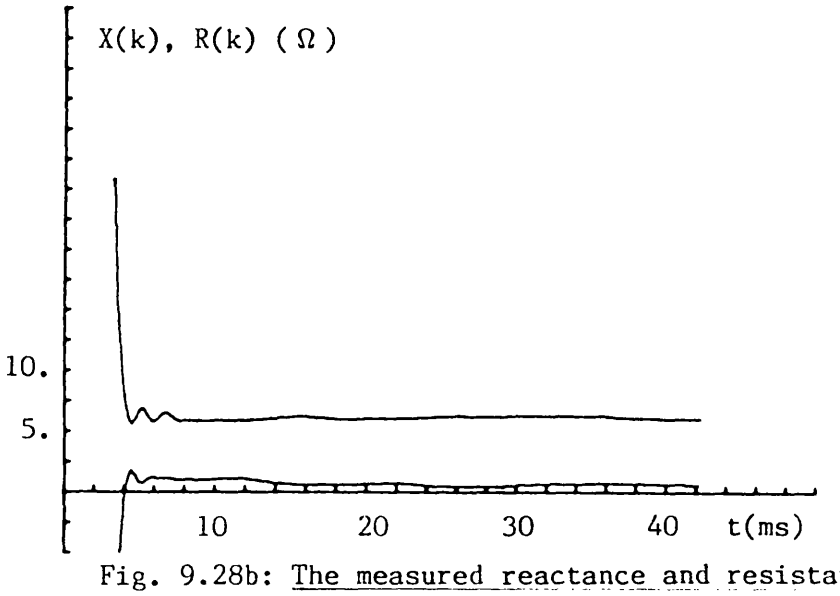


Fig. 9.28b: The measured reactance and resistance for the fault condition of Fig. 9.28a.

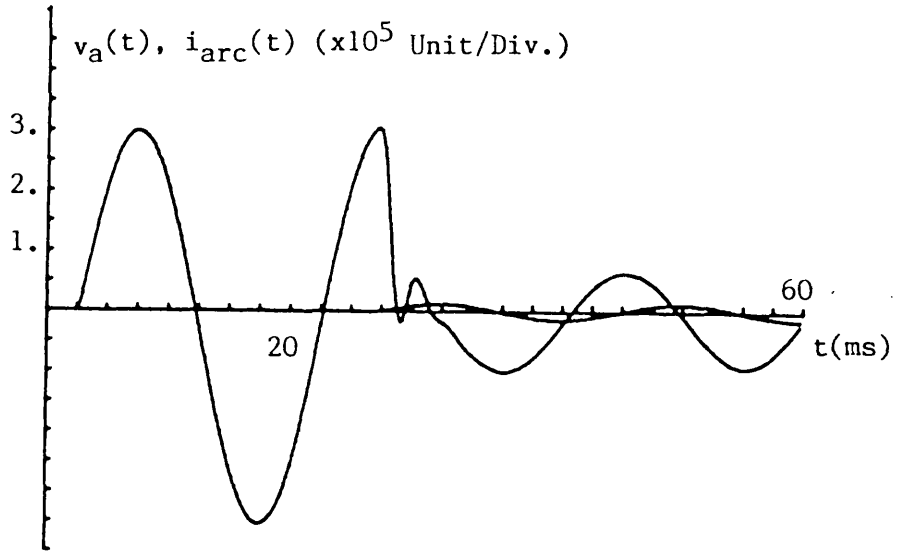


Fig. 9.29a: Voltage and current signals for a fault at 19.2 km, 90 degree inception angle and SIR of 4.7.

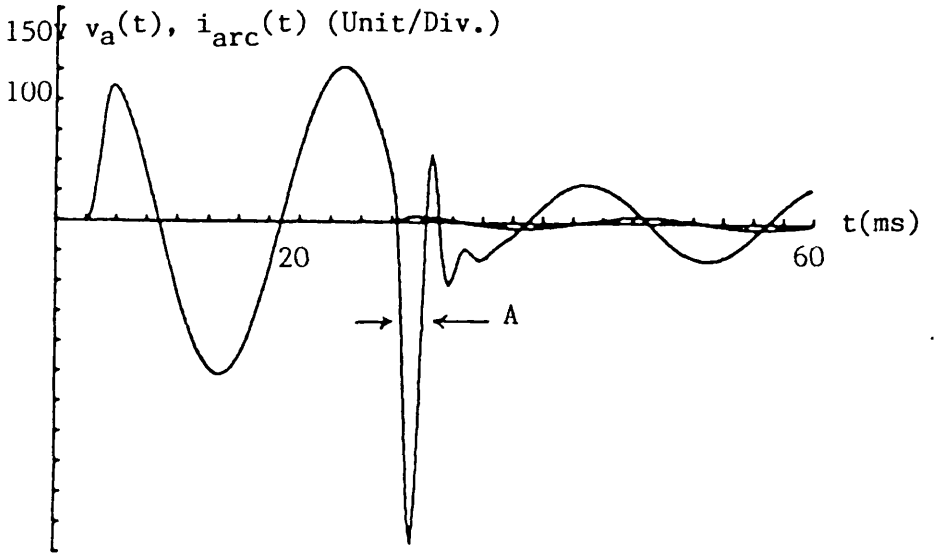


Fig. 9.29b: The output of the pre-conditioning filter which shows a long downward droop in the phase voltage. Fault conditions of Fig. 9.29a.

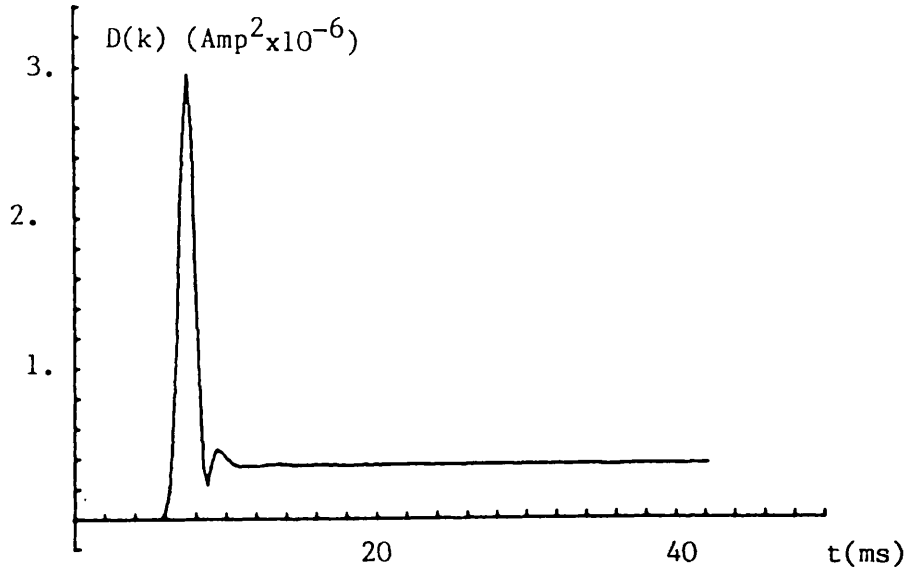


Fig. 9.30a: The behaviour of D(k) for a fault at the relay reach (24 km line) and SIR of 4.6, 90 degree fault inception angle.

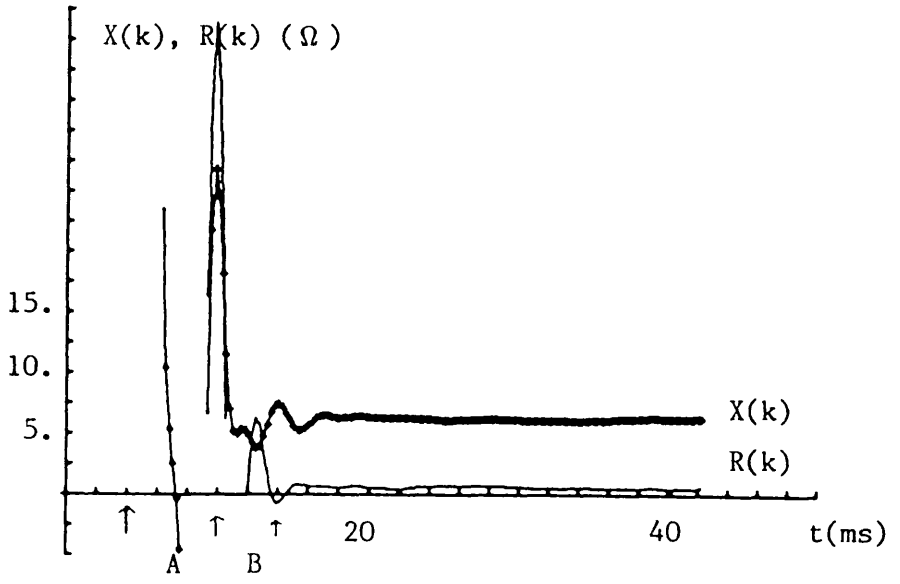


Fig. 9.30b: The measured reactance and resistance for the fault condition of Fig. 9.30a.

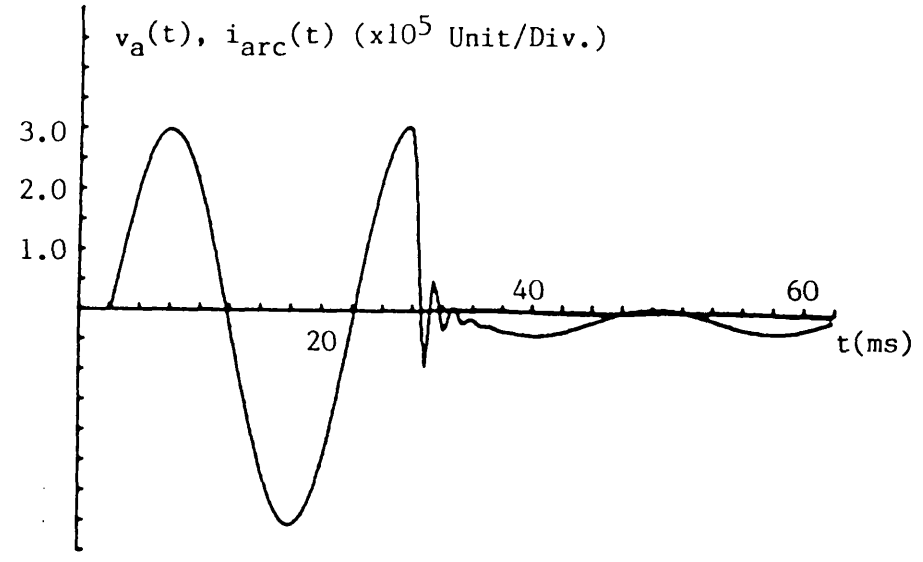


Fig. 9.31a: The voltage and current signals for a fault at 19.2 km, 90 degree inception angle and SIR of 23.

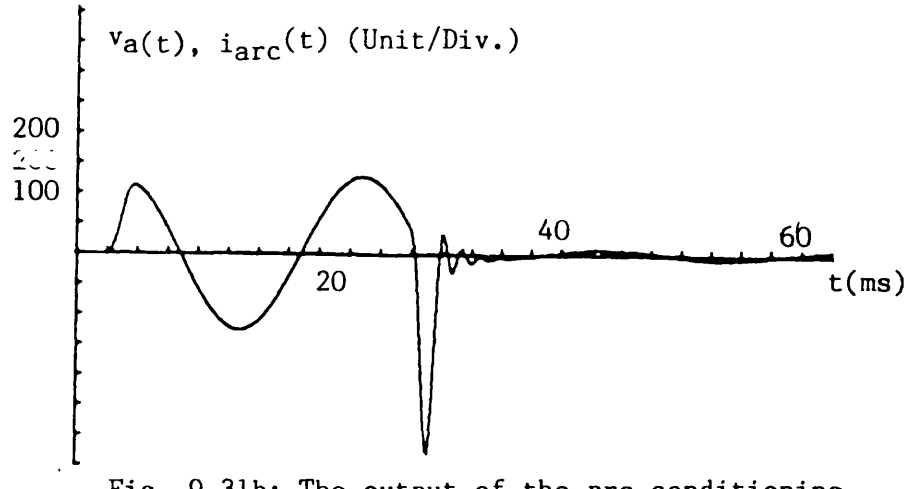


Fig. 9.31b: The output of the pre-conditioning filter for the fault condition of Fig. 9.31a.

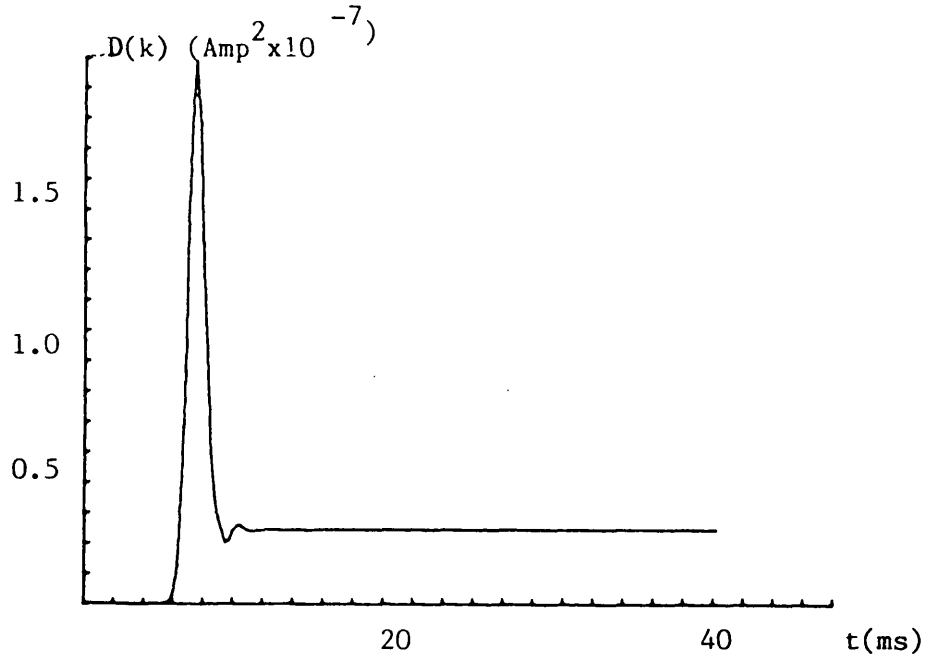


Fig. 9.32a: The behaviour of D(k) for the fault codition of Fig. 9.31a.

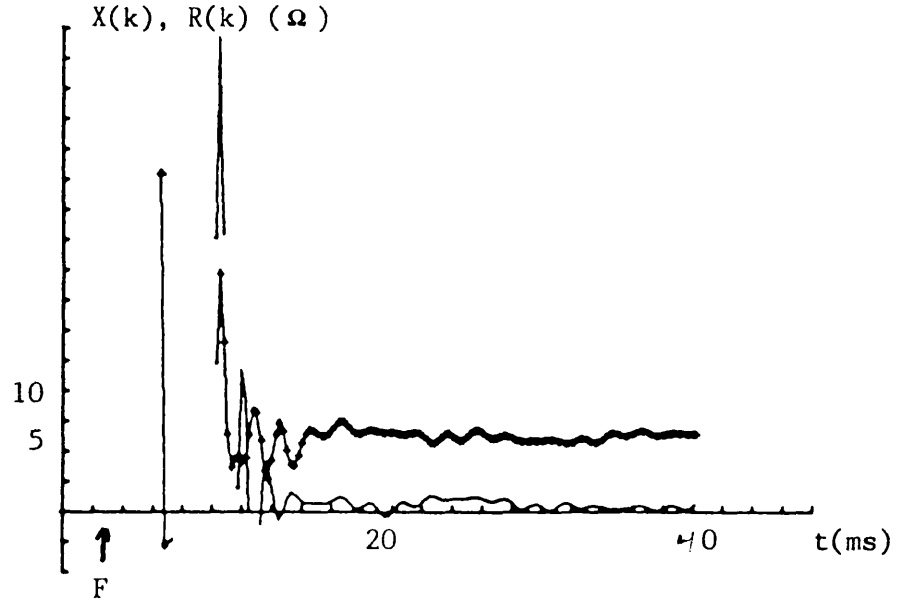


Fig. 9.32b: The measured reactance and resistance for the fault condition of Fig. 9.31a.

X(k)

R(k)

CHAPTER 10

SUMMARY OF WORK, CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

10.1 SUMMARY OF WORK

The work described in this thesis concerns the development of a new u.h.s. relay, based on the finite Fourier Transform of a short data window. The distance protection algorithm is a modification of the basic algorithm which relates the Fourier Transform of a finite data window of information derived from the measurands of the fault loop impedance, as described in Chapter 4. The advantage of this technique is the flexibility of the window width T_w, through which the scheme may look at the relaying signals. For practical purposes two transformation windows were selected, 6 ms and 2 ms. For the finite Fourier Transform process, the extraction frequency is also arbitrary, but for practical purposes it was found that $f_e = 1/2T_w$ is the optimum extraction frequency, since this maximises the magnitude of the determinant term D(k).

In order to implement the process algorithm, a conventional hardware structure was used. The latter consisted of an advanced data acquisition unit, a Z8002 16-bit microcomputer and a multiplier unit incorporating a fast hardware multiplier. The data acquisition unit consisted of FIR filters, a 16-channel analogue multiplexer, a 12-bit A/D converter and a direct memory access unit (DMA). For the realization of the FIR filters, use was made of charge-coupled-device (CCD) tapped delay lines. The analogue multiplexed Fourier Transform components were converted to 12-bit digital format and transferred through a DMA unit to the Z8002

microcomputer unit. The Z8002 microcomputer manipulated the data and formed the vector multiplier buffer, which was transferred through a programmable DMA unit to the multiplier chip.

In order to achieve a consistent relay operating time, the algorithm was implemented using a discrete signal processing technique. In this technique the relaying signal samples were fed to the process for individual measurand estimation.

For the algorithm implementation, a quadrilateral characteristic was adopted and a trip signal was initiated when the measurands converged inside this region. A trip criterion based on a single impedance estimate could lead to the degradation in protection integrity because, in practice, significant fluctuations in the impedance estimates occur after fault inception. In order to maintain the relay reach accuracy, a decision logic process incorporating an up and down counter was used. The counter is incremented when the measurands fall within the protected zone characteristic and decremented for out of zone measurements.

The relay performance was investigated using PTL equipments, from which a series of waveforms corresponding to various types of fault, for different line configurations, was applied. The relaying voltage signals were processed through a CVT simulation program using parameters derived from an actual CVT frequency response. The CT simulation was not undertaken, since the CT frequency response was of relatively wider band width when compared with that of the anti-aliasing filter, which was set to have a cut-off frequency of 2 kHz.

In order to achieve a greater accuracy, the voltage and current transformed components were set to have equal level, for a fault at the relay reach.

The relay was tested for the 6 ms and 2 ms transformation windows. For the 6 ms window, a 128 km line was used, using local source capacities of 5 GVA and 35 GVA. Lumped parameter primary system simulation fault waveforms were applied for solid faults at 0, 45, 90 and 135 degree inception angles, together with primary system waveforms for various resistive faults, at 0 and 90 degree inception angles. The relay directional stability was tested, using the principles of the directional stability, for a one cycle voltage memory bank. For the 2 ms window, the relay was tested by applying solid faults for 128 km and 24 km transmission lines. For low level signal conditions, the relay was tested using the 24 km line and SIR values of up to 23. For various SIR, the relay reach accuracy was tested and a level threshold was applied for the process implementation.

10.2 CONCLUSIONS

A distance protection relay was successfully designed and tested. The relay tests showed that u.h.s. performance can be achieved, using the finite Fourier Transform. The relay speed is affected by the transformation window width. As shown in Chapter 8, using a 6 ms transformation window, for a 128 km line, the relay operating time ranges between 7 ms to 10 ms, for faults between 0% and 80% of the relay reach. For the 2 ms transformation window, the relay operating time ranges between 4 ms to 7.5 ms for the same fault conditions, as shown in Chapter 9. The slow response of the relay for the 6 ms transformation window is

due to the fact that this window has the first zero in the frequency response occurring at 250 Hz, whereas the 2 ms transformation window has the first zero at 700 Hz. For u.h.s. distance protection, the frequency response of the relaying signal filters is of vital importance, since it determines the speed of the relay. As a rule, the more limited the band width of frequency transmitted by a filter, the more extended in time is its impulse response. This is just a reflection of the general antithesis between the frequency selectivity and impulse response. The significance of this rule manifests itself in the design of filters for power system protection relays, where a highly selective filter with a sharp pass band yields a slow response to a fault, consequently leading to a slow operation, as with the 6 ms transformation window.

For resistive faults, the observed relay operating time becomes slower as the fault resistance increases. For close-up faults the resistive coverage of the relay was found to be 40 Ω. For power system protection relays this is a desirable feature, since close-up faults can have the greatest de-stabilizing effect upon the system. However, the relay resistive coverage deteriorates for highly resistive faults with high source capacities at the remote end, where the quadrilateral characteristic truncates. In practice, e.h.c. line faults involve a relatively low arc resistance, thus similar relay operating times when compared with the solid fault response. The relay operating times for resistive faults and the relay performance assessments are described fully in Section 8.10.

As mentioned previously, the internal fault current signal is set to

have a level equal to that of the voltage signal, for a fault at the relay reach. Thus, for close-up faults, with a high source capacity at the relaying point, clipping in the current signal is unavoidable. It was observed that when the clipping persists for longer than 1 ms, the decision logic counter starts to decrement indicating an out of zone fault. For the 128 km line, 35 GVA source capacity at the relaying point, the decision logic counter reaches a trip level of + 5 counts before clipping persists (8-9 counts). However, for longer lines and high source capacities at the relaying end, one cycle fault clearance is questionable. Moreover, the restriction of the trip level by the current clipping and the decrement of the decision logic counter for faults well inside the protected zone boundary represents undesirable features. Therefore, it is essential to provide the relay with clip detection facilities which upon detecting a clip in the current signals, causes the decision logic counter to be incremented. This is possible because current clipping is a definitive in zone fault condition. The clip detection technique is described in Section 10.3.4.

In order to maintain the relay directional integrity, the directional reactance $(X_m(k))$ technique was implemented. As described in Section 8.11, this technique uses the delayed samples of the transformed voltage in conjunction with the undelayed samples of the transformed current components. The technique was implemented by using a voltage memory bank, which holds the samples of one cycle of the transformed voltage components. For reverse faults, the directional reactance prevents relay operation. However for reverse close-up faults, the relay responds to a fault as the voltage memory bank runs out of the pre-fault samples. This is due to the complete collapse in the phase voltage and

the CVT transient, since the CVT relaxation time causes low frequency components to penetrate the process. Therefore, the samples of more than one pre-fault cycle of the voltage transformed components must be used, as necessitated by operational requirements. For forward faults, the directional reactance constraint is satisfied rapidly and the relay operating time is not affected, with the exception of close-up faults up to 35% of the relay reach, 0 degrees inception angle and 35 GVA source capacity at the relaying end. For these types of fault, the directional reactance maintains a negative magnitude which indicates a reverse fault for approximately 10 ms. As the directional reactance term converges to a positive magnitude, indicating a forward fault, it coincides with the severe current clipping, which causes the decision logic counter to decrement. In order to remedy this problem a clip detection technique must be used and as clipping is detected the decision logic counter is incremented, thus overriding the decision logic process and the directional reactance constraint.

The conventional hardware structure, used for implementing the process imposes a speed limitation on the relay sampling rate. The speed limitation is due to the loading of the multibus by the peripherals, the data acquisition unit and the multiplier unit, since there are continuous requirements for the bus acquisition which requires arbitration according to the peripheral priority.

The realization of the FIR filters was made by using the CCD tapped delay lines, which proved to be unreliable for the algorithm implementation. One of the main factors is the dynamic range limitation, which has a S/N ratio of -50 dB. Moreover, a problem in accurately setting the

filter coefficients was encountered.

In order to overcome the problems associated with the CCD filters and the processing speed limitations, a more advanced hardware structure must be used, such as TMS320 signal processing systems and a master 16-bit processor, as described in Section 10.3.1.

The relay reach accuracy was tested for 128 km and 24 km lines. For a 90 degree inception angle, the relay overreach deteriorates as the SIR increases. The relay overreach is caused by two factors. Firstly, the D(k) differencing noise, which causes random decision logic counter increments for a fault beyond the relay reach at high SIR. Secondly, product truncation errors, where only the most significant 16-bit of the 32-bit product are retrieved. Consider a fault at SIR of 30, where for a fault at the relay reach, the relaying signals are represented by 55 conversion levels (16 Vp.p nominal input). The 55 conversion levels occupy the 6 least significant bits of the 12-bit A/D converter. Internal to the relay, each word is shifted by 4-bits; thus the relaying signal information is contained in the 10-least significant bits of the 16-bit processor. The 10-bit multiplication process produces 20-bit products, so that only the 4 most significant bits of the products are retrieved, which proved to be inadequate for maintaining accurate relay reach.

As stressed throughout this work, the relaying term D(k) is sensitive to the relaying current exponential offset. For a pure sinusoidal current signal, D(k) has a d.c. magnitude. In the event of the relaying current exponential offset, D(k) develops a sinusoidal component imposed

on the steady state level and, under strong offset conditions, D(k) can achieve a negative value, and the constraints involving D(k) are not satisfied. The algorithm simulation studies show that the reduction of the exponential offset by about 50% maintains a unipolar D(k). However, this produces a considerable overreach problem as described in Section 9.9.2. Therefore, it is essential to remove the exponential offset before the algorithm is implemented.

Under low level signal conditions, the relay noise has a considerable impact on the reach accuracy, and therefore the relay operation must, in such situations be restrained. As described in Section 9.14.2, the relay operation was inhibited for a fault at the relay reach for SIR of 17, since over 20% overreach was observed. Two techniques were used to inhibit the relay operation, the first of which was to measure the magnitude of D(k) for the latter fault (average magnitude of 12 conversion levels), from which a D(k) threshold of 14 conversion levels was set. When the measured D(k) magnitude is smaller than 14 conversion levels, the measurement is regarded as unreliable and the decision logic counter is decremented. The second technique was to set a level threshold for the voltage and current transformed components for the latter described fault. As mentioned previously, the transformed components have an equal level for a fault at the relay reach. Thus, a similar threshold level can be applied to both voltage and current transformed components. Moreover, the negative part of the transformed components can be inverted, thus allowing comparison against the positive level threshold only. It was found that a relay sensitivity of 9% is adequate to maintain a satisfactory reach accuracy, as shown in Section 9.15. The use of the level threshold does not affect the relay

operating time at low SIR. However, it was observed that the relay operating time becomes inconsistent for faults at a SIR of 17.

In order to improve the relay reach accuracy for 0 degree inception angle faults, a digital preconditioning filter was utilized, which is a breakthrough for the algorithm implementation. The filter has infinite attenuation in the frequency response at 0 Hz, thus the exponential offset is virtually eliminated. The filter has a set of zeros at frequencies of 600 Hz and above to attenuate the travelling wave components. For 0 degree inception faults the relay performance is considerably improved, and the simulated measured reactance converges to a steady state post-fault magnitude rapidly. For 90 degree inception angle faults, the measured reactance converges to the post-fault magnitude rapidly and fast operating characteristics are maintained. However, for faults at the relay reach, the measured reactance converges to a transient magnitude smaller than that of the steady state post-fault reactance. This was of particular concern for a fault at the relay reach at low SIR, typically SIR of 5, where the transient downward droop in the measured reactance is observed to be for 3 ms. For higher SIR values, the reactance transient downward droop is of less significance and the decision logic process is capable of preventing relay overreach. Nevertheless, an accurate relay reach can be achieved for all practical SIR values by using a dynamic trip level decision logic process as described in Section 10.3.3.

10.3 SUGGESTIONS FOR FUTURE WORK

10.3.1 Relay hardware structure

Although the implementation of the algorithm, for a full three phase scheme is technically possible, however this may lead to economically unviable hardware. Moreover, recent developments in digital signal processing technique makes it possible to utilize more efficient and faster relay hardware. In order to overcome the CCD filter limitations, consideration was given to the use of TRW multiplier accumulator (MAC) chips, which perform 16-bit multiplication and accumulation in typically 300 ns. The use of the MAC will improve the realization of the process digital filtering, but it will not reduce the burden on the processor unit, since a considerable time is consumed on data manipulation and basic operations such as add, subtract and shift. Thus more advanced systems, which provide digital filtering facilities and the basic processing instructions are considered, of which the TEXAS TMS320 signal processing system is an example. The TMS320 is a full signal processing system which contains ROM, RAM, ALU and a hardware multiplier on one chip, thus ideally suited for the algorithm implementation. The TMS320 has a limited instruction set, which is optimized for signal processing tasks, and is provided with multiply, accumulate and data shift instruction which execute in 200 ns. Thus, for a typical FIR filtering process, 400 ns is required for each stage (load a sample, multiply with a coefficient, accumulate and shift the sample to the next location in the data memory). The add and subtract instructions execute in 200 ns.

In order to realize the algorithm digital filtering as proposed in Section 10.3.2, the 12-stage digital preconditioning filter executes

in 4.8 μs. The sine and cosine convolution filters, for a 1.5 ms transformation window execute in 4.8 μs. However, to include the time required to load the new samples and to retrieve the filtering signals from the accumulator, the time required to realize the filtering functions is 12 μs, for each of the relaying signals. Thus for a full three phase scheme, a total of 72 ms is required to filter the signals. Since each of the relaying signal filters execute in 12 μs, the process can be arranged such that following the completion of each signal filtering, the A/D converter must complete the conversion of the next signal; thus a conversion time of 10 μs is ideally suited. As described in Section 10.3.2, it is proposed to use additional digital filtering to smooth the D(k) differencing noise and a 6 stage digital filter is suggested. Thus to filter D(k), $LD(k)/T_s$, RD(k) and $L_m D(k)/T_s$ 9.6 μs is required for each type of fault. For a full three phase scheme, an estimated time of 57.6 μs is therefore required. The overall time required for the digital filtering is then estimated to be 129.6 μs. This time represents 51% of the processing time for a 4 kHz processing cycle. The intermediate filter storage occupies 140 words of the available 144 word RAM. Thus a limitation would arise from a storage point of view. In this respect it must be noted that the filter coefficients can be stored in the program memory and accessed directly by the TMS320 multiplier. In order to reduce the requirement for intermediate data storage, the current transformed components $i_1(k-1)$ and $i_2(k-1)$ required for D(k) evaluation and the phase voltage transformed components $v_1(k-N)$ and $v_2(k-N)$ required for the directional reactance can be stored in external memory, since the TMS320 can provide a support for up to 4 kbyte of external memory. The filtered relaying signals are transferred to a master processor, which must be a fast 16-bit microcomputer,

with a system timer counter to perform the task of providing timing waveforms to synchronise the relay hardware operations and to perform the decision logic process. The task of transferring the 18 relaying terms must be accomplished in less than 20% of the processing cycle, to allow a sufficient time for the decision logic process. Since a general purpose processor performs the transfer of 16-bit data in approximately 6 μs, which consumes 43% of the processing cycle. Therefore it is proposed to use a DMA controller chip such as HITACHI (HD68450), which transfers a 16-bit word in 500 ns, resulting only 5% of the processing cycle being consumed.

The proposed relay hardware structure consists of sample and holds, strobed at 4 kHz, an analogue multiplexer scanned at 24 kHz, a 10 μs conversion cycle 12-bit A/D convertor, a TMS320 and a 16-bit microcomputer with DMA interface. Fig. 10.1 shows the proposed relay hardware block diagram.

10.3.2 Digital filtering optimization

In realizing the finite Fourier Transform, a digital preconditioning filter with unity coefficients was employed. The choice of the unity coefficients was made to simplify the filter practical realization, since the process merely requires add, subtract and shift. However, the use of unity coefficients inherits the behaviour of rectangular windows, where the side loops are bigger when compared with other windowing types. Moreover, the realization of the filtering functions using the TMS320 is independent of the coefficient magnitude, since multiply, add and subtract execute in 400 ns. The proposed digital preconditioning filter takes the transfer function of Eqn. 10.1.

$$H(z) = 0.309\ z^{-1}(1 + z^{-5} - z^{-6} - z^{-11}) + 0.587\ z^{-2}(1 + z^{-3} - z^{-6} - z^{-9})$$
$$+ 0.809\ z^{-3}(1 + z^{-1} - z^{-6} - z^{-7}) \quad \text{--- } 10.1$$

Figs. 10.2 and 10.3 show the filter impulse and frequency responses respectively. As shown in Fig. 10.3, the filter has infinite attenuation in the frequency response at 0 Hz, which is essential to eliminate the relaying current exponential offset. The filter provides over 20 dB attenuation for the frequencies ranging between 600 Hz to 2 kHz.

In order to implement the algorithm, it is required to extract the Fourier Transform components. The phase modified Fourier Transform component filter transfer functions take the form of Eqns. 10.2 and 10.3.

$$H_1(z) = z^{-1} + 0.702\ z^{-2} + 0.26\ z^{-3} - 0.26\ z^{-4} - 0.702\ z^{-5} - z^{-6} \quad \text{--- } 10.2$$

$$H_2(z) = 0.25\ z^{-1} + 0.7\ z^{-2} + z^{-3} + z^{-4} + 0.7\ z^{-5} + 0.25\ z^{-6} \quad \text{--- } 10.3$$

The filter impulse responses are shown in Fig. 9.16a.

One of the problems encountered in the algorithm implementation, is the D(k) digital differencing noise. Therefore a D(k) smoothing process is proposed. As shown in Appendix 11, the frequency response of a digital differencer is expressed in the form of Eqn. 10.4.

$$|H(j\omega)| = [2(1 - \text{COS } n\omega T_s)]^{1/2} \quad \text{--- } 10.4$$

where $|H(j\omega)|$ is the magnitude of the frequency response at frequency ω, and n is the number of stages employed by the digital differencer. The frequency responses of one and 5-stage differencers are shown in

Fig. A11.1. For the two sample differencer, the frequency components, in particular the high frequency components, are accentuated. The 5-stage differencer provides a set of zeros in the frequency response at 0 Hz, 800 Hz, 1.6 kHz, 2.4 kHz, 3.2 kHz and 4 kHz. Nevertheless, frequency components between the frequency response zeros are accentuated. Therefore, the differencing noise must be filtered. From the test observations, the differencing noise is generally of a high frequency nature, and as shown in Chapter 9, an analogue filter with 3 dB attenuation at 500 Hz was adequate to attenuate D(k) differencing noise. Therefore, a 6-stage digital filter with a transfer function taking the form of Eqn. 10.5 is proposed.

$$H(z) = z^{-1}(1 + z^{-5}) + 0.74\ z^{-2}(1 + z^{-3}) + 0.85\ z^{-3}(1 + z^{-1}) \quad \text{---} \quad 10.5$$

The impulse response of the filter is shown in Figs. 10.4 and 10.5 shows the filter frequency response. The first zero in the frequency response occurs at 620 Hz, and all frequencies above are attenuated by over 12 dB. It must be noted that this digital filter is applied to all the decision logic terms, D(k), $LD(k)/T_s$, RD(k) and $L_m D(k)/T_s$.

The preliminary effects of the digital filters on the relay performance are studied in two areas. Firstly, the effect of the 6-stage smoothing filter on the reactance term behaviour, and secondly the effect of the proposed digital filtering on the relay performance.

Case 1 : The effect of the smoothing filter on the relay performance

The effect of the 6-stage low pass filter is studied in conjunction with the unity coefficient filter (as described in Section 9.16). For all types of fault tested, with 128 km and 24 km lines, the filter

introduces less than 1 ms delay. Fig. 10.6 shows the behaviour of the measured reactance for a fault at 35% of the relay reach, 128 km line, 90 degree inception angle and local source capacity of 5 GVA. The delayed filtered reactance converges to the post-fault value in less than 1 ms when compared with the unfiltered reactance term. Fig. 10.7 shows the effect of filtering X(k) for a fault at 100% of the relay reach, where the fluctuation in the post-fault reactance is considerably reduced. Figs. 10.8 and 10.9 show the reactance behaviour for a close-up fault and a fault at the relay reach for SIR of 5, 24 km line, respectively. Similar test observations are obtained when compared with the latter described 128 km line faults.

Case 2 : The effect of the proposed digital filtering on the relay performance

The effect of the new 12-stage digital filtering and the 6-stage digital smoothing filter is studied with a particular reference to faults at the relay reach. Fig. 10.10 shows the behaviour of the reactance term for a fault at the relay reach for 128 km line, 5 GVA local source capacity and 90 degree inception angle. The reactance term (unfiltered) shows less fluctuation when compared with that of the unity coefficients filter Fig. 10.7. The filtered reactance term shows a smooth pattern when compared with its equivalent, Fig. 10.7. A similar observation is obtained using a 24 km line, for various SIR. Fig. 10.11 shows the behaviour of the reactance term for a fault at the relay reach with an SIR of 5.

10.3.3 Dynamic trip level decision logic process

As described in Sections 9.17 and 10.3.2, the measured reactance suffers a downward droop for faults at the relay reach at high SIR, with a 90

degree inception angle. This is of particular concern at SIR of 5, since the transient downward droop in the measured reactance is of approximately 3 ms (8-10 counts), and can cause considerable overreach. However, to fix the decision logic process trip level on about 16 counts introduces unwanted delay in the relay operating time. Alternatively, a dynamic trip level decision logic process can be adopted, with 8 and 16 count trip levels. The 8 count trip level is used for faults up to 75% of the relay reach, where the decision logic counter is characterized by increments of 2 (inner zone region). When the decision logic counter increments by 1 for 3 measurements, the trip level is incremented to 16 counts. With respect to the implementation of the decision logic process, it is suggested that two counters are used, a main counter and an auxiliary counter which holds the history of the increments by 1. As the main counter reaches 8 counts, the auxiliary counter is tested. When it holds 3 or more counts, the trip level is incremented to 16, otherwise a trip signal is initiated. With respect to measurements outside the protected zone, the main counter is decremented by 2. Following a trip signal initiation the auxiliary counter reset to 0.

10.3.4 Digital clip detection

As mentioned previously, current clipping causes an error in the decision logic process, which decrements for faults well inside the protection zone boundary. However, for a 128 km line, close-up fault, the decision logic counter reached the trip level before the current clipping persisted (8-9 counts). For longer lines, current clipping for a close-up fault is more severe and as such results in slower relay operation. Moreover, the restriction of the trip level because of the current

clipping was considered an undesirable feature. In order to detect current clipping, the clipping level can be arranged to be (+ and - 2048 conversion levels). The current signal is compared against a clip level threshold (CLT), which is set to be around 4 conversion levels below the clip level. When the compared current signals exceed the CLT, the measurement is treated unreliable and the decision logic main counter is incremented by 2. In order to ensure that the relay signal processing is linear for faults between 80% to 100% of the relay reach, the setting can be modified such that the voltage and current signals have equal level for a fault at 80% of the relay reach, with no clipping permitted at this setting. However, if overreach problems are encountered because of the clip detection technique, the rate of change of the relaying current can be incorporated. Theoretically, when clipping occurs, the rate of change in the current signal is zero. In practice, the difference between two successive samples in the event of clipping is (+ and - LSB). Thus if the comparison against the CLT is satisfied and the difference between two successive samples is less than 3 conversion levels, a current clip condition is satisfied and the decision logic main counter is incremented by 2.

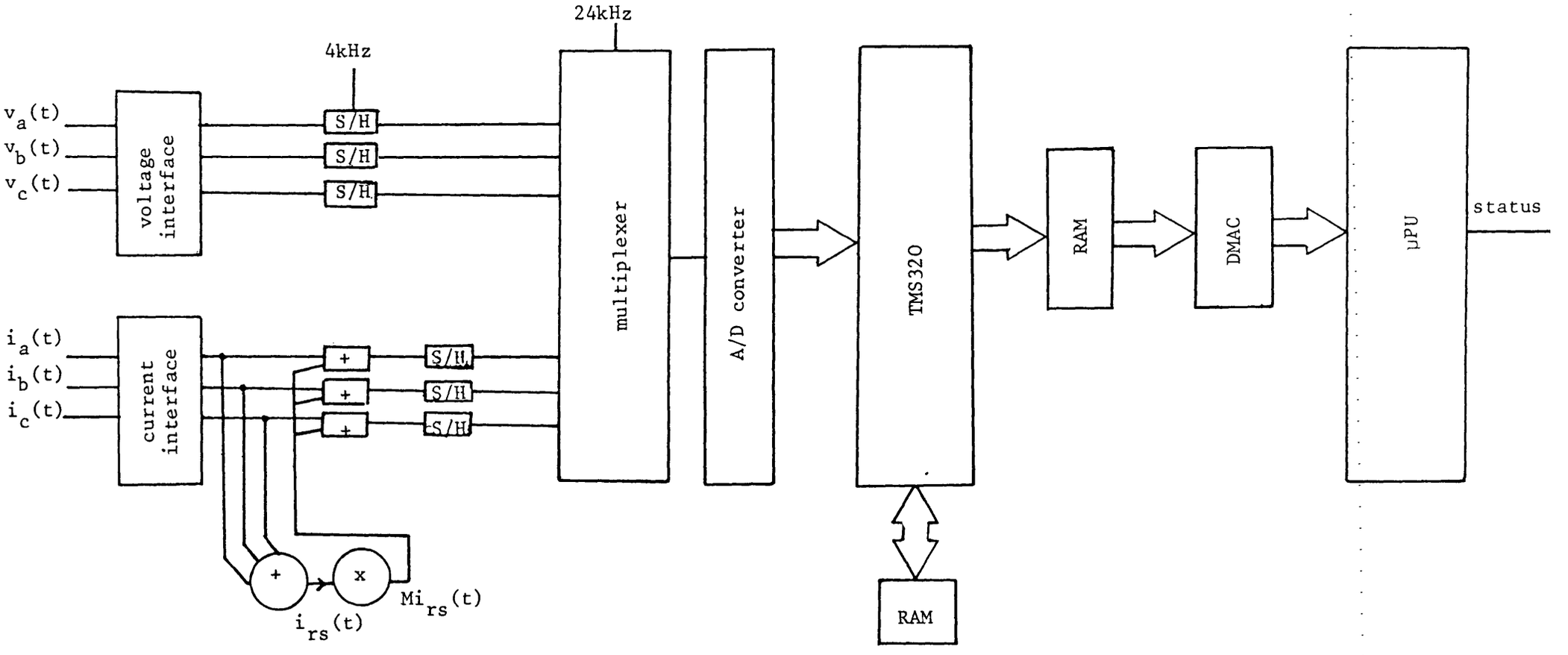


Fig. 10.1 : Proposed relay hardware

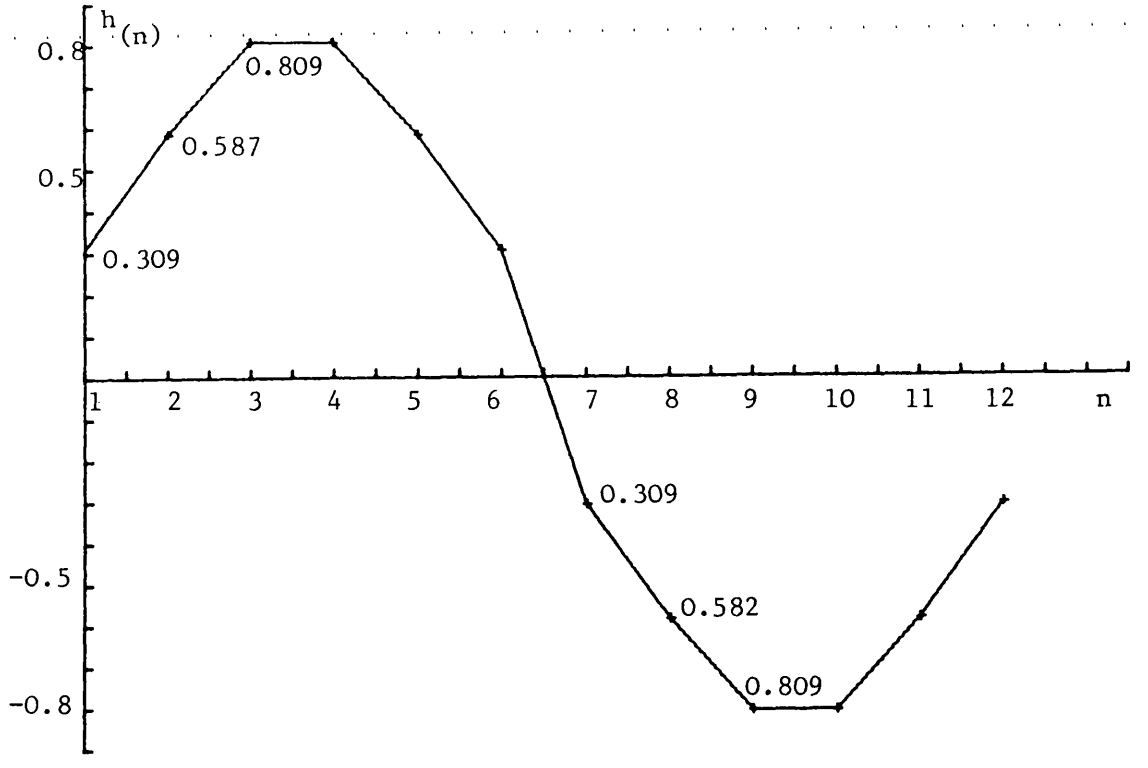


Fig. 10.2 : Pre-conditioning filter impulse response

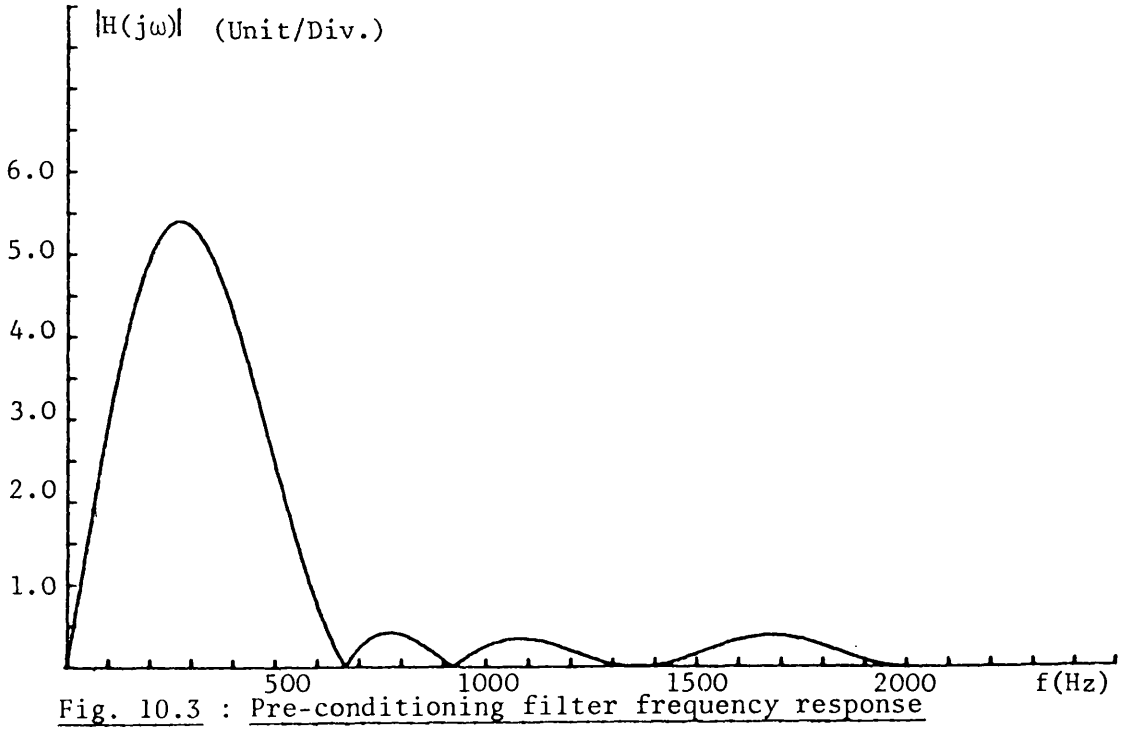


Fig. 10.3 : Pre-conditioning filter frequency response

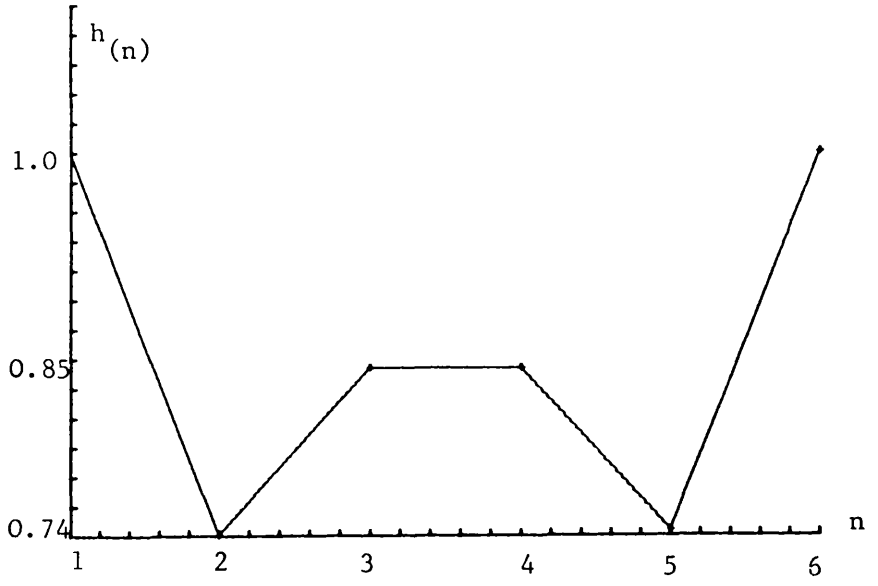


Fig. 10.4 : Smoothing filter impulse response

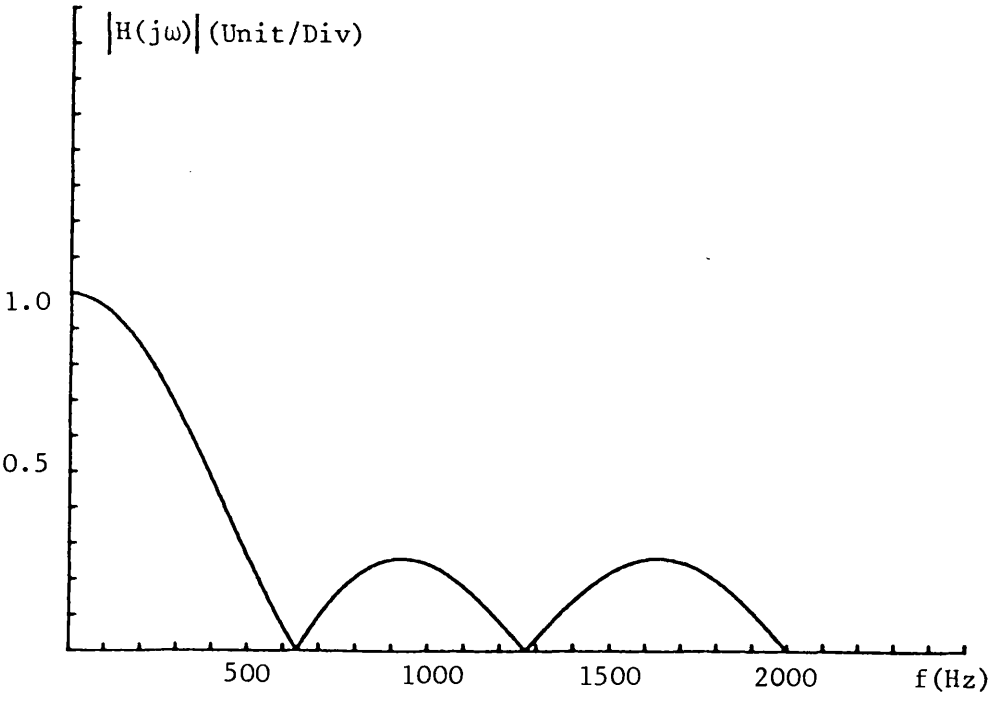


Fig. 10.5 : Smoothing filter frequency response

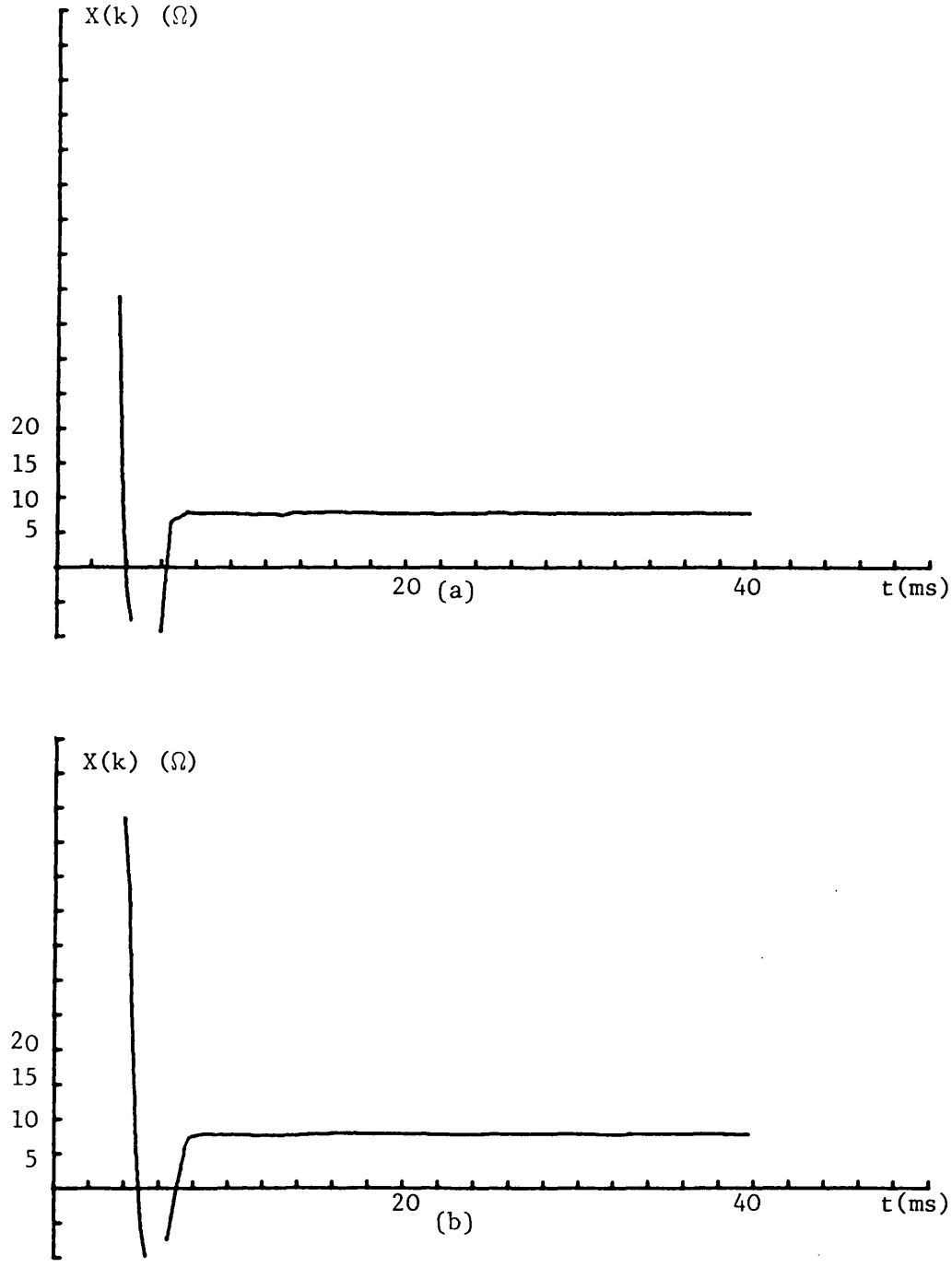


Fig. 10.6 : The behaviour of X(k) for a fault at 35% of the relay reach (128 km line), 90 degree inception angle, 5 GVA source capacity of the relaying end and 35 GVA source capacity of the remote end

(a) using the unity pre-conditioning filter
(b) filtered X(k) using the smoothing filter of Fig. 10.4

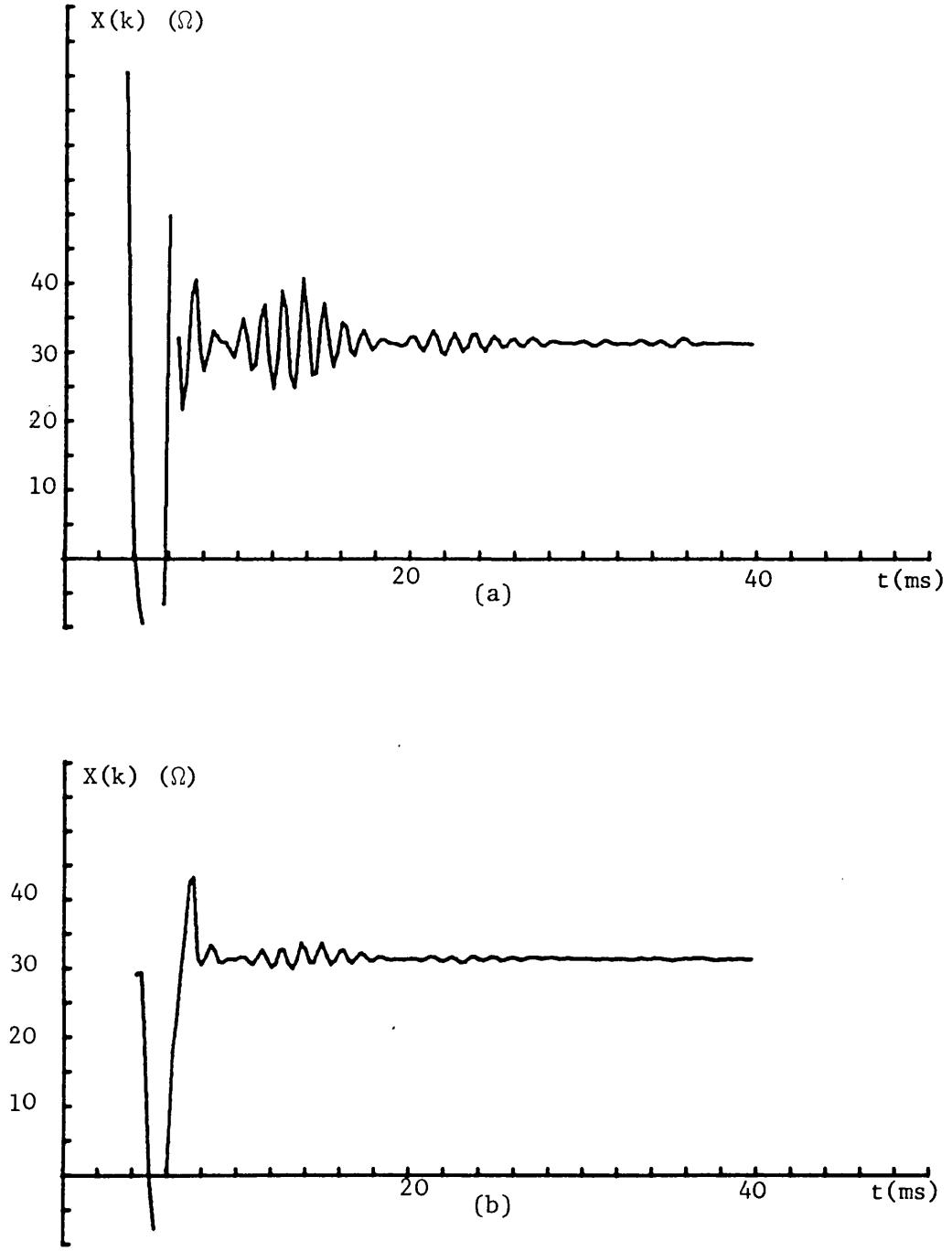


Fig. 10.7 : The behaviour of X(k) for a fault at the relay reach (128 km line), 90 degree inception angle, 5 GVA source capacity at the relaying end and 35 GVA source capacity at the remote end

(a) using the unity coefficient pre-conditioning filter
(b) filtered X(k) using the smoothing filter of Fig. 10.4

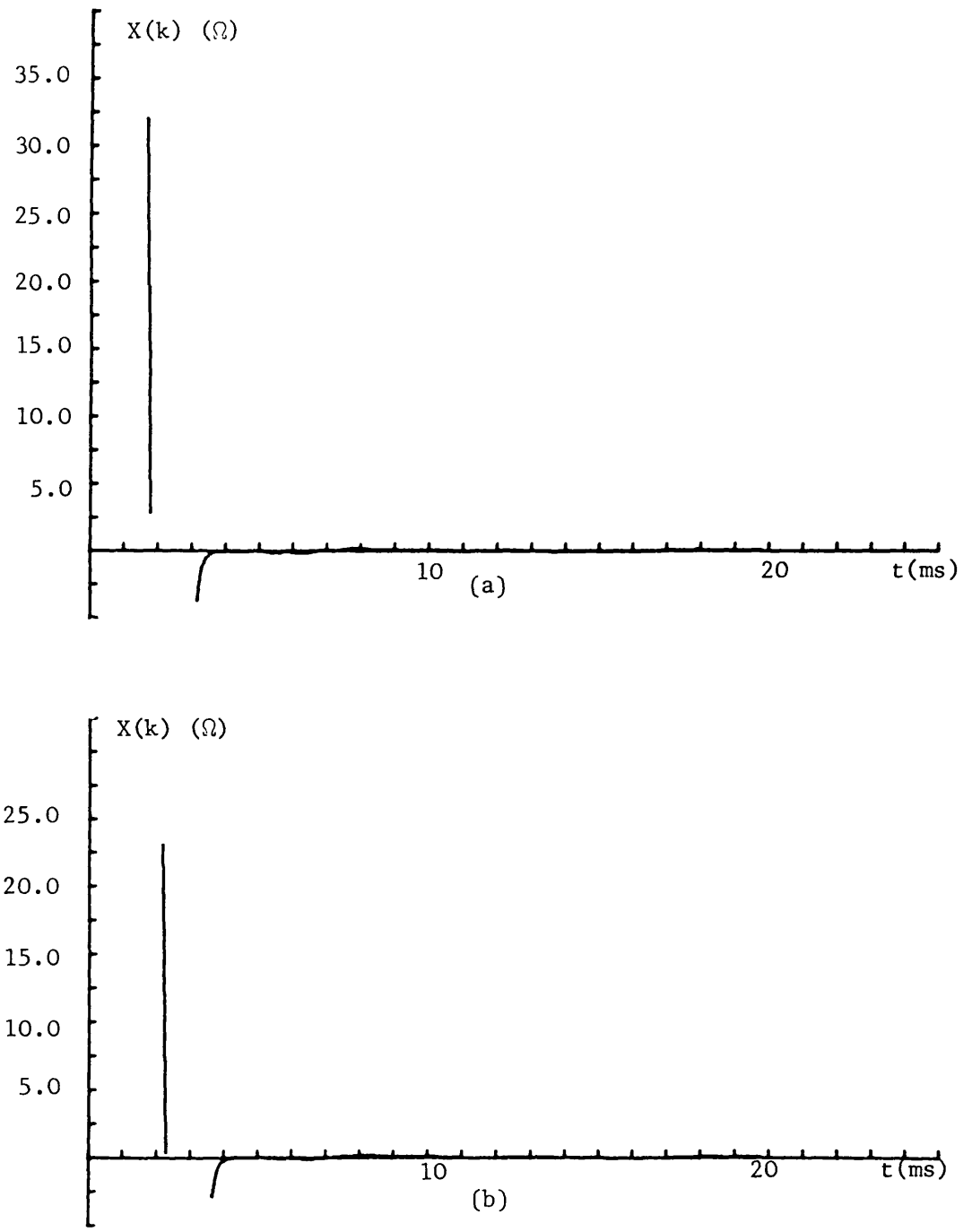


Fig. 10.8 : The behaviour of X(k) for a close-up fault (24 km line), 90 degree inception angle and SIR of 4.6

(a) using the unity coefficient pre-conditioning filter
(b) filtered X(k) using the smoothing filter of Fig. 10.4

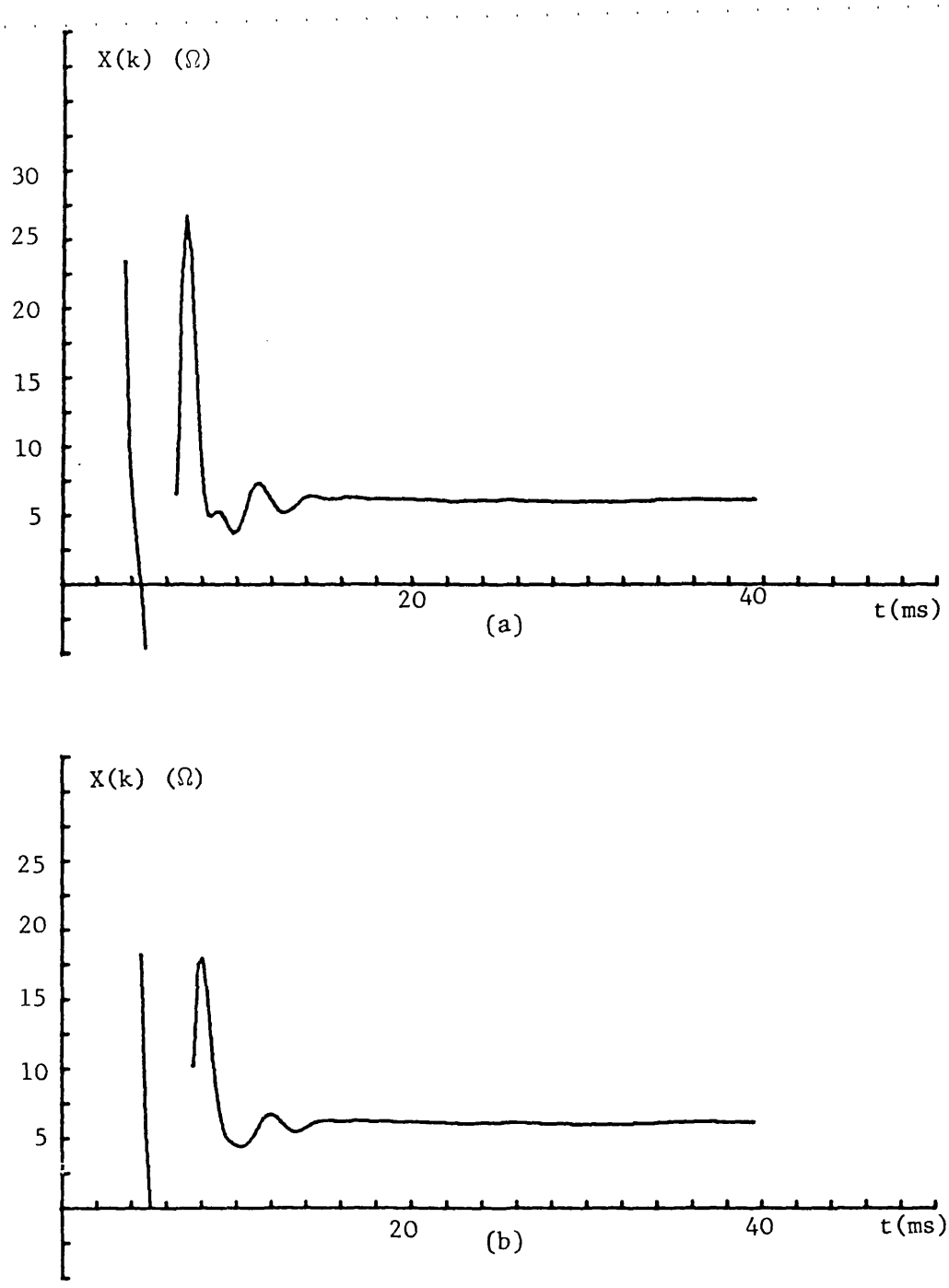


Fig. 10.9 : The behaviour of X(k) for a fault at the relay reach (24 km line), 90 degree inception angle and SIR of 4.6

(a) using the unity coefficients pre-conditioning filter
(b) filtered X(k) using the smoothing filter of Fig. 10.4

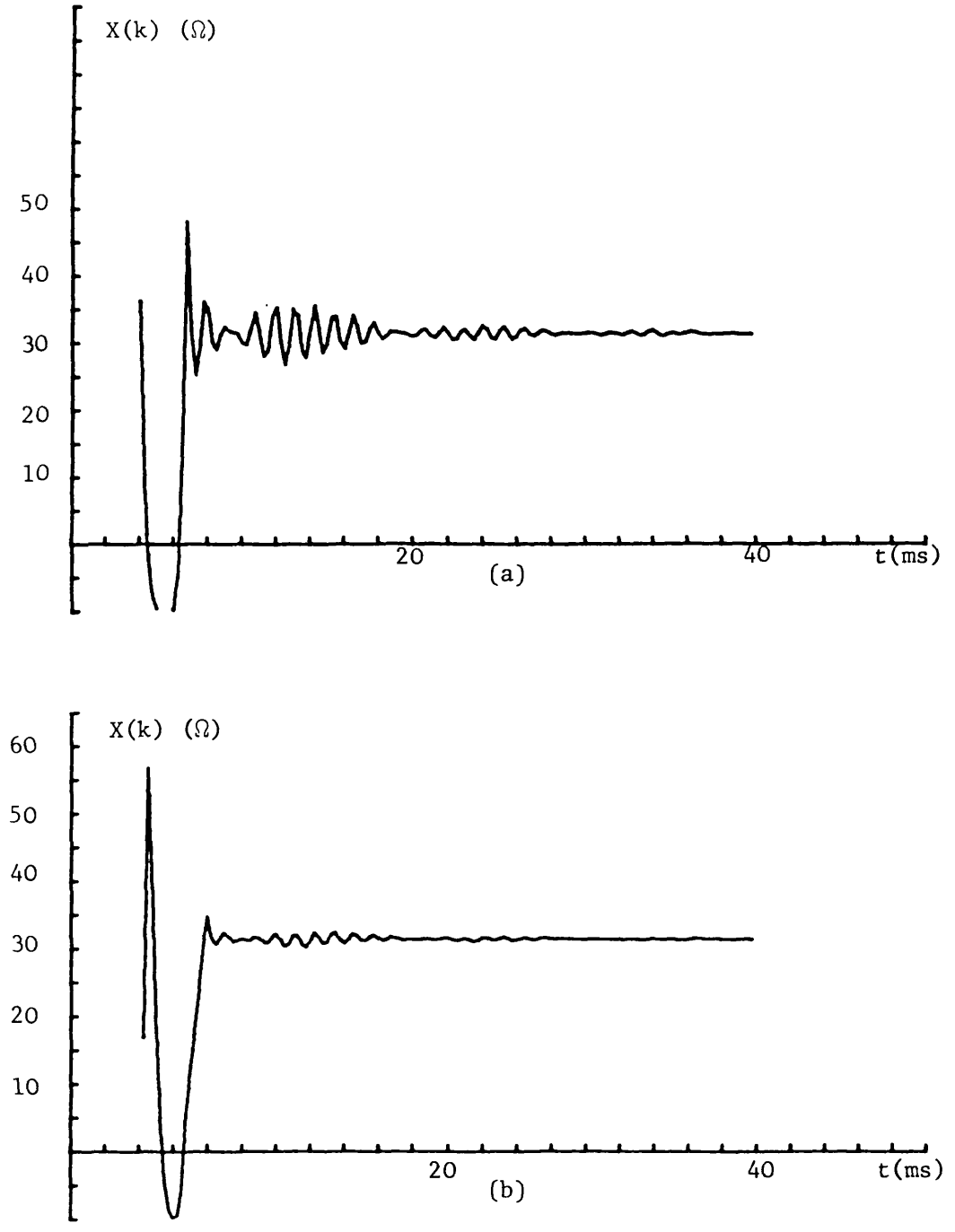
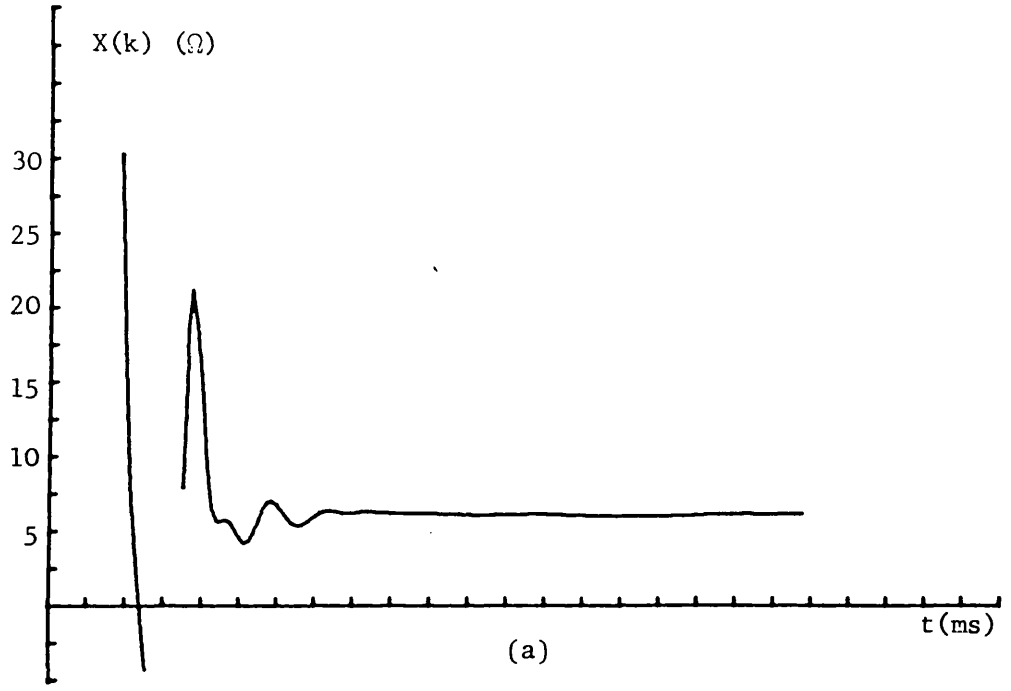


Fig. 10.10 : The behaviour of X(k) for a fault at the relay reach (128 km line), 90 degree inception angle, 5 GVA source capacity at the relaying end and 35 GVA source capacity at the remote end

(a) using the pre-conditioning filter of Fig. 10.2
(b) filtered X(k) using the smoothing filter of Fig. 10.4



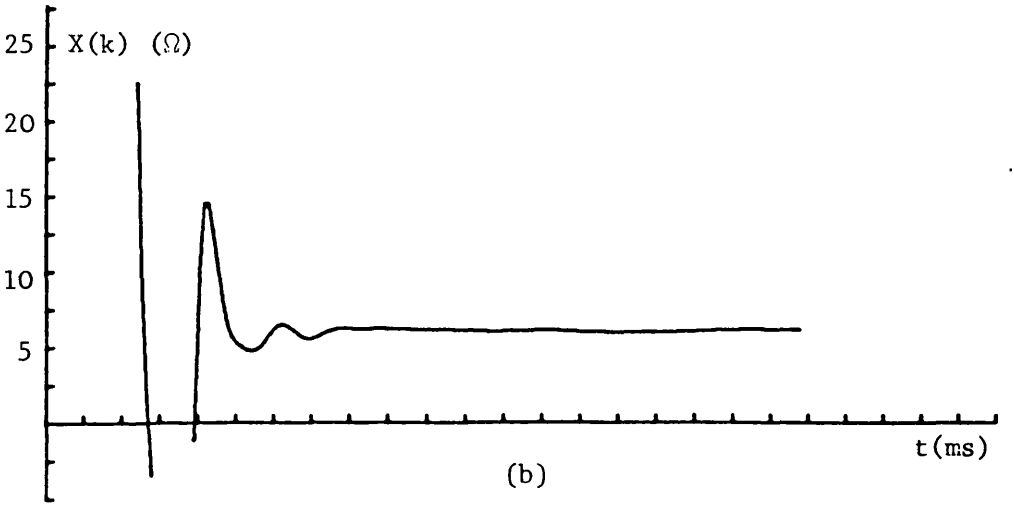


Fig. 10.11 : The behaviour of X(k) for a fault at the relay reach (24 km line), 90 degree inception angle and SIR of 4.6

(a) using the pre-conditioning filter of Fig. 10.2
(b) filtered X(k) using the smoothing filter of Fig. 10.4

APPENDIX 1

RESIDUAL CURRENT COMPENSATION

Distance protection relay impedance measurements make use of the voltages and currents at the relaying point. In practice, the effects of the earth return have to be considered when estimating the phase sequence impedance. Furthermore, the mutual effects of other circuits must be accounted for.

Consider a single phase earth fault in phase "a" as shown in Fig. A1.1. Under this fault condition the relaying voltage $v_a(t) = i_a(t)\ Z\ell + i_{rs}(t)\ Zg$. If the relay fed with voltage $v_a(t)$ and current $i_a(t)$, the relay measures an impedance equivalent to $Z\ell + Zg$, while it is set to cover a distance specified by $Z\ell$. It will be seen that the relay will measure an impedance $Z\ell$ if it is fed with current equal to the phase current plus the scaled residual current of expression A1.1.

$$i_{rs}(t) = i_a(t) + i_b(t) + i_c(t) \qquad \text{--- A1.1}$$

Consider a transposed overhead line system, having a self impedance $Z_{s\ell}$ and mutual impedance Z_m. The voltage drop in the conductor may be represented by the following matrix expression.

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} Z_{s\ell} & Z_m & Z_m \\ Z_m & Z_{s\ell} & Z_m \\ Z_m & Z_m & Z_{s\ell} \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \qquad \text{--- A1.2}$$

For a phase to earth fault at distance (α) from the feeder, $v_a(t)$ can be expressed in the form:

$$v_a(t) = \alpha[Z_{s\ell}\ i_a(t) + Z_m\ i_b(t) + Z_m\ i_c(t)] \qquad \text{--- A1.3}$$

which, using expression A1.3, rearranges to the form of Eqn. A1.4.

$$v_a(t) = \alpha\ (Z_{s\ell}-Z_m) \left\{ i_a(t) + \left(\frac{Z_m}{Z_{s\ell}-Z_m} \right)\ i_{rs}(t) \right\} \qquad \text{--- A1.4}$$

For an overhead line:

$$Z\ell_1 = Z\ell_2 = Z_{s\ell}-Z_m \qquad \text{--- A1.5}$$

where $Z\ell_1$ and $Z\ell_2$ are the positive and negative phase sequence impedance respectively, and the zero phase sequence impedance $Z\ell_0$ is given by Eqn. A1.6.

$$Z\ell_0 = Z_{s\ell} + 2Z_m \qquad \text{--- A1.6}$$

From Eqns. A1.5 and A1.6 the mutual impedance is given by Eqn. A1.7.

$$Z_m = \frac{1}{3}\ (Z\ell_0-Z\ell_1) \qquad \text{--- A1.7}$$

Applying Eqns. A1.6 and A1.7 to Eqn. A1.4 gives:

$$v_a(t) = \alpha Z\ell_1 \left\{ i_a(t) + \frac{1}{3} \left(\frac{Z\ell_0-Z\ell_1}{Z\ell_1} \right)\ i_{rs}(t) \right\} \qquad \text{--- A1.8}$$

$$v_a(t) = \alpha Z\ell_1\ [i_a(t) + M\ i_{rs}(t)] \qquad \text{--- A1.9}$$

where M is the residual current compensation factor, given by Eqn. A1.10.

$$M = \frac{1}{3} \left(\frac{Z\ell_0}{Z\ell_1} - 1 \right) \qquad \text{--- A1.10}$$

For a typical 400 kV line, $Z\ell_1$ and $Z\ell_0$ are given by:

$$Z\ell_1 = 0.01726 + j0.2873\ ,\ |Z\ell_1| = 0.287818\ \Omega/km$$

$$Z\ell_0 = 0.10380 + j0.8673\ ,\ |Z\ell_0| = 0.873489\ \Omega/km$$

From Eqn. A1.7, Z_m evaluates to:

$|Z_m| = 0.195\ \Omega/km$

And from Eqn. A1.5, $Z_{s\ell}$ evaluates to:

$|Z_{s\ell}| = 0.483\ \Omega/km$

and using Eqn. A1.11, M evaluates to 0.678.

For phase a-b fault, the relaying voltage is given by:

$$v_{ab}(t) = \left(v_a(t) - v_b(t)\right) \qquad \text{--- A1.11}$$

where $v_a(t) = \alpha Z\ell_1 \left(i_a(t) + Mi_{rs}(t)\right)$ and $v_b(t) = \alpha Z\ell_1 \left(i_b(t) + Mi_{rs}(t)\right)$.
Eqn. A1.11 leads to the following form:

$$v_{ab} = \alpha Z\ell_1 \left(i_a(t) - i_b(t)\right) \qquad \text{--- A1.12}$$

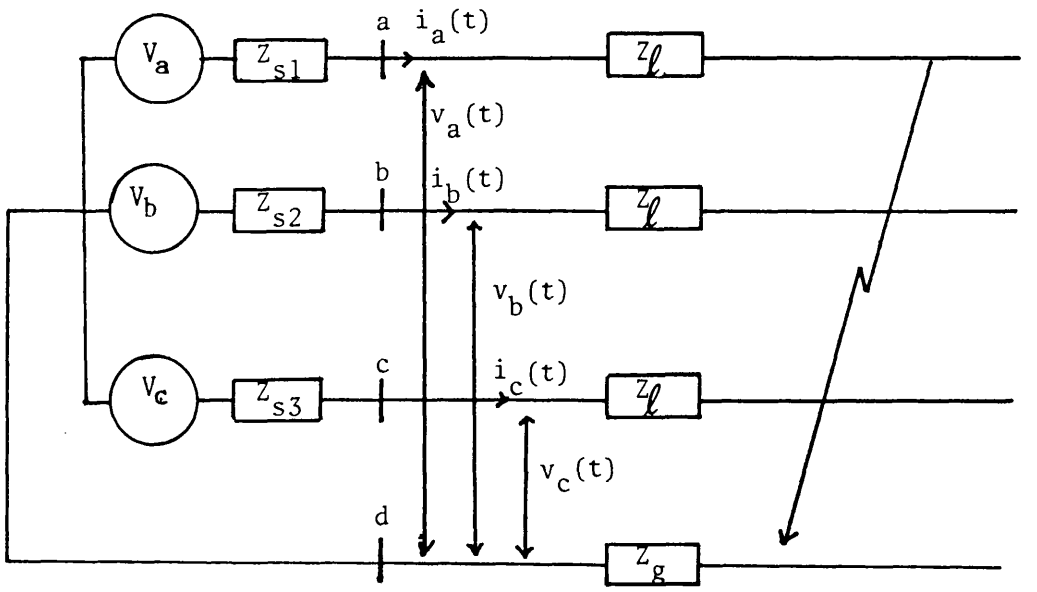


Fig. A1.1 : Single phase-earth fault system representation

APPENDIX 2

QUADRILATERAL CHARACTERISTIC CONSTANTS K_3, K_4 and K_5

NUMERICAL EVALUATION

From Appendix 8 it can be seen that the relay voltage and current data scaling are as follows.

$$K_v K_{vt} = 1/39191.836 \quad \text{--- A2.1}$$

$$K_c K_{ct} = 1/1332.19 \quad \text{--- A2.2}$$

For typical 400 kV line, the $Z\ell_1$ is 0.2873 ohm/km. For a 102.4 km relay reach, corresponding to 80% of 128.0 km line length, the line p.p.s. impedance at the reach point is given by Eqn. A2.3.

$$Z\ell_1 = 0.2873 \times 102.4 = 29.419 \quad \text{--- A2.3}$$

The scaled impedance Z_{rs} at the reach point is given by Eqn. A2.4.

$$Z_{rs} = Z\ell_1 \frac{K_v K_{vt}}{K_c K_{ct}} = 0.999 \quad \text{--- A2.4}$$

For a 50 Hz system and using a 2.7 kHz sampling rate, then

$$\frac{1}{\omega_0 T_s} = 8.44 \quad \text{--- A2.5}$$

From Eqns. 4.37 ($K_4 = X_r/\omega_0 T_s$), A2.4 and A2.5, K_4 evaluates to:

$$K_4 = 8.43$$

From Eqn. 4.36, K_3 is given by:

$$K_3 = \frac{X_0}{\omega_0 T_s}$$

where X_0 is 1.5 ohm, thus the scaled X0, i.e. X_{0s} is given by:

$$X_{0s} = X_0 \frac{K_v K_{vt}}{K_c K_{ct}} = 0.05 \qquad \text{--- A2.6}$$

therefore K_3 is given by:

$$K_3 = -0.429$$

From Eqn. 3.38, K_5 is given by:

$$K_5 = K_1 \omega_0 T_s$$

where K_1 = COT86 = 0.069, therefore K_5 is given by:

$$K_5 = 0.008$$

It must be noted that all the constants in the Eqns. 4.34 and 4.35 are obtained from the processor arithmetic shift instructions. For example K_4, which is approximated to 8.5, can be derived as:

8.5D(K) = 8D(K) + 0.5D(K) = arithmetic left shift by 3 bits + arithmetic right shift by one bit.

APPENDIX 3

THE BEHAVIOUR OF D(t)

Consider the relay current signals $I_1(t)$ and $I_2(t)$ derived from convolution integrals as follows:

$$i_1(t) = \int_0^{T_w} i(t-\tau)\, h_1(\tau)\, d(\tau) \qquad \text{--- A3.1}$$

$$i_2(t) = \int_0^{T_w} i(t-\tau)\, h_2(\tau)\, d(\tau) \qquad \text{--- A3.2}$$

The convolution integrals can be expressed in the frequency domain by applying the Fourier Transform as follows:

$$\mathcal{F}[i_1(t)] = I_1(\omega_0) = I(\omega_0)\, H_1(\omega_0) \qquad \text{--- A3.3}$$

$$\mathcal{F}[i_2(t)] = I_2(\omega_0) = I(\omega_0)\, H_2(\omega_0) \qquad \text{--- A3.4}$$

Application of the shift theorem to define the previous sample $(t-T_s)$ which is required for calculation of the D(t) terms gives the following Eqns.:

$$\mathcal{F}[i_1(t-T_s) = I(\omega_0)\, H_1(\omega_0)\, EXP(-j\omega_0 T_s) \qquad \text{--- A3.5}$$

$$\mathcal{F}[i_2(t-T_s) = I(\omega_0)\, H_2(\omega_0)\, EXP(-j\omega_0 T_s) \qquad \text{--- A3.6}$$

Case 1 : Steady state sinusoidal input

Consider a steady sinusoidal input of the form:

$$i(t) = I_p\, COS(\omega_0 t + \theta_1) \qquad \text{--- A3.7}$$

The present and previous current samples can be expressed as:

$$i_1(t) = |H_1(\omega_0)|\ I_p\ COS(\omega_0 t + \theta_1 + \phi_{11}) \quad \text{--- A3.8}$$

$$i_2(t) = |H_2(\omega_0)|\ I_p\ COS(\omega_0 t + \theta_1 + \phi_{12}) \quad \text{--- A3.9}$$

$$i_1(t-T_s) = |H_1(\omega_0)|\ I_p\ COS(\omega_0 t + \theta_1 + \phi_{11} - \omega_0 T_s) \quad \text{--- A3.10}$$

$$i_2(t-T_s) = |H_2(\omega_0)|\ I_p\ COS(\omega_0 t + \theta_1 + \phi_{12} - \omega_0 T_s) \quad \text{--- A3.11}$$

where ϕ_{11} and ϕ_{12} are the phase shift of the filters $H_1(\omega_0)$ and $H_2(\omega_0)$ respectively:

$$H_1(\omega_0) = |H_1(\omega_0)|\ \underline{\lfloor \phi_{11}} \quad \text{--- A3.12}$$

$$H_2(\omega_0) = |H_2(\omega_0)|\ \underline{\lfloor \phi_{12}} \quad \text{--- A3.13}$$

Using Eqn. 4.24 gives:

$$D(t) = |H_1(\omega_0)|\ |H_2(\omega_0)|\ I_p^2\ COS(\omega_0 t + \theta_1 + \phi_{11} - \omega_0 T_s)\ COS(\omega_0 t + \theta_1 + \phi_{12})$$
$$- |H_1(\omega_0)|\ |H_2(\omega_0)|\ I_p^2\ COS(\omega_0 t + \theta_1 + \phi_{11})\ COS(\omega_0 t + \theta_1 + \phi_{12} - \omega_0 T_s)$$
$$\text{--- A3.14}$$

Using the identity $COS(A)\ COS(B) = \frac{1}{2}\ [COS(A-B) - COS(A+B)]$, D(t) gives:

$$D(t) = |H_1(\omega_0)|\ |H_2(\omega_0)|\ \frac{I_p^2}{2}\ [COS(\phi_{11} + \phi_{12} - \omega_0 T_s)$$
$$+ COS(2\omega_0 t + 2\theta_1 + \phi_{11} + \phi_{12} - \omega_0 T_s) - COS(\phi_{11} - \phi_{12} - \omega_0 T_s)$$
$$- COS(2\omega_0 t + \phi_{11} + \phi_{12} - \omega_0 T_s)] \quad \text{--- A3.15}$$

Using the identity $2\ SIN(A)\ SIN(B) = COS(A-B) - COS(A+B)$ gives:

$$D_{ss} = D(t) = |H_1(\omega_0)|\ |H_2(\omega_0)|\ I_p^2\ SIN(\phi_{11} - \phi_{12})\ SIN(\omega_0 T_s) \quad \text{--- A3.16}$$

Case 2 : d.c. Offset condition

Consider a d.c. offset sinusoidal input in the form:

$$i(t) = a_0 + I_p \, COS(\omega_0 t + \theta_1) \quad \text{--- A3.17}$$

where a_0 is the exponential offset component. The present and previous current samples can be expressed as:

$$i_1(t) = a_{01} + I_p \, |H_1(\omega_0)| \, COS(\omega_0 t + \theta_1 + \phi_{11}) \quad \text{--- A3.18}$$

$$i_2(t) = a_{02} + I_p \, |H_2(\omega_0)| \, COS(\omega_0 t + \theta_1 + \phi_{12}) \quad \text{--- A3.19}$$

$$i_1(t-T_s) = a_{01} + I_p \, |H_1(\omega_0)| \, COS(\omega_0 t + \theta_1 + \phi_{11} - \omega_0 T_s) \quad \text{--- A3.20}$$

$$i_2(t-T_s) = a_{02} + I_p \, |H_2(\omega_0)| \, COS(\omega_0 t + \theta_1 + \phi_{12} - \omega_0 T_s) \quad \text{--- A3.21}$$

where $a_{01} = a_1 \, H_1(\omega_0)$ --- A3.22

$a_{02} = a_1 \, H_2(\omega_0)$ --- A3.23

Using the previous approach gives:

$$\begin{aligned} D(t) = {} & |H_1(\omega_0)| \, |H_2(\omega_0)| \, I_p^2 \, SIN(\phi_{11} - \phi_{12}) \, SIN(\omega_0 T_s) \\ & + a_1 \, a_{01} \, |H_2(\omega_0)| \, COS(\omega_0 t + \theta_1 + \phi_{12}) \\ & + a_1 \, a_{02} \, |H_1(\omega_0)| \, COS(\omega_0 t + \theta_1 + \phi_{11} - \omega_0 T_s) \\ & - a_1 \, a_{01} \, |H_2(\omega_0)| \, COS(\omega_0 t + \theta_1 + \phi_{12} - \omega_0 T_s) \\ & - a_1 \, a_{02} \, |H_1(\omega_0)| \, COS(\omega_0 t + \theta_1 + \phi_{12}) \end{aligned} \quad \text{--- A3.24}$$

$$D(t) = [D_{ss}] + [D_{off}] \quad \text{--- A3.25}$$

The term D_{ss} is the auto-product for a sinusoidal input as given by Eqn. A3.26, and D_{off} is the sinusoidal component derived from the d.c. offset.

APPENDIX 4

DISTANCE PROTECTION ACCURACY

Distance protection specification requires a 5% reach accuracy for faults up to system impedance ratio (SIR) of 30, where

$$SIR = \frac{Z_{s1}}{Z\ell_1} \quad . \qquad \text{--- A4.1}$$

Consider the equivalent circuit for 3-phase to earth fault shown in Fig. A4.1. The relay voltage input (V_r) for Fig. A4.1 is given by Eqn. A4.2.

$$V_r = \frac{Z\ell_1}{Z\ell_1 + Z_{s1}} Ea \qquad \text{--- A4.2}$$

Eqn. A4.2 can be written as:

$$V_r = \frac{1}{1 + Z_{s1}/Z\ell_1} Ea \qquad \text{--- A4.3}$$

If Ea has a nominal value of 63.5 Vrms, and for an SIR = 30, V_r becomes:

$$V_r = \frac{63.5}{1 + 30} = 2.05 \text{ Vrms} \qquad \text{--- A4.4}$$

Eqn. A4.4 implies that the relaying voltage can vary from 63.5 Vrms secondary to 2.05 Vrms for fault with SIR of 30. However, from network operation and earthing considerations, relays should be designed for maximum input relaying signals of 150%, i.e. 95.25 Vrms. Consider a minimum input signal of 2.05 Vrms, which gives signals variation (Vmin/Vmax) of 0.0215. The relay must be sensitive to 5% of the relaying signals at SIR = 30, and the relay sensitivity (S) is therefore given by:

$$S = 0.05 \times 0.0215 = 0.0016 \quad \text{--- A4.5}$$

The relay dynamic range can be expressed in dB as:

$$\text{Dynamic range (dB)} = -20 \log S = -59.37 \text{ dB} \quad \text{--- A4.6}$$

The result obtained by Eqn. A4.6 implies that the errors and noise within the measurement should be limited to a level compatible with the above sensitivity. For the analogue components of the relay, consideration must be given to the use of devices with signal to noise ratio of at least -60 dB. For the digital process, in order to represent a 60 dB dynamic range, the digital process requires 2^n quantization levels, as given by Eqn. A4.7.

$$\text{Dynamic range (dB)} = -20 \log(2)^n \quad \text{--- A4.7}$$

where n is the number of bits. Therefore for dynamic range of 60 dB, n must be higher than 9. For practical purposes, A/D converters are available in 8, 12 and 14 bits, thus 12-bits has been chosen. Similarly microcomputers are available in 8 and 16 bits, thus 16-bit processor has been chosen.

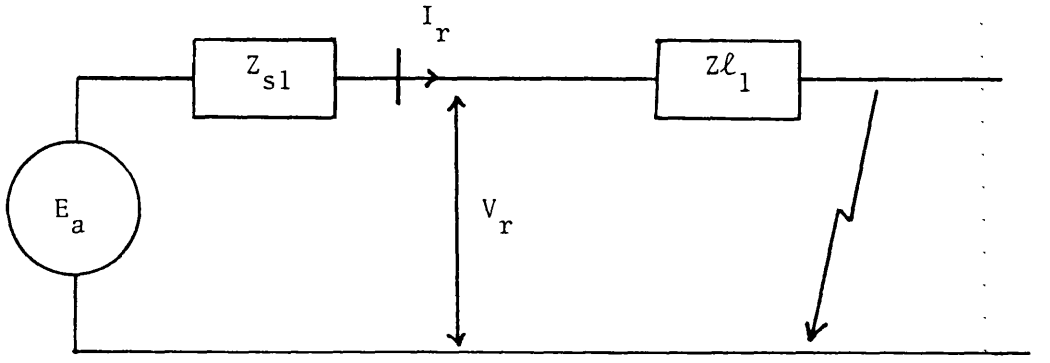


Fig. A4.1 : Equivalent circuit for three phase-earth fault network

APPENDIX 5

PROCESSOR AND MULTIPLIER UNIT TECHNICAL DESCRIPTION

A5.1 Z8002 DOWNLOAD TECHNICAL DESCRIPTION

A software assembler package was provided for the PDP 11/23. The function of the assembler was to convert a source program consisting of a sequence of assembly language instructions into an object code binary format, executable by the CPU. As the assembler package assembled a program, a source listing file and an object code file in octal format was generated. The download program read the object code file and transferred it to a specific destination within the Z8002 RAM memory. The object code file was provided with key binary code as follows.

Address code (204)

Instruction code (200)

End of file (220)

Fig. A5.1 shows the Z8002 download flow chart.

A5.2 MULTIBUS EXCHANGE SIGNALS

The bus exchange logic unit uses a discrete logic process, prior to a DMA cycle, for the bus acquisition. To perform the required bus exchange process, five exchange signals are used, Bus Clock (BCLK*), Bus Busy (BUSY*), Bus Priority In (BPRN*), Bus Priority Out (BPRO*) and Common Bus Request (CBRQ*). Note that the (*) means active low command. The bus exchange must be synchronized with BCLK*, with the synchronization occurring with the falling edge of the 50% duty cycle pulse. The BCLK* has a frequency of 9.5 MHz.

BUSY* is a command driven by the bus master in control of the bus. When a master asserts BUSY*, the BUSY* signal prevents other bus masters from gaining control of the bus. Another master is allowed to access the bus after the bus master in control of the bus deactivates its BUSY*, to indicate the completion of its access.

The bus priority commands, BPRN* and PBRO* are used to resolve the masters priority. Active BPRN* indicates that no master of higher priority is requesting the bus. When the master request the bus it activate BPRO* to inform lower priority masters that a higher priority master bus request exists. In a serial priority scheme, the highest priority BPRO* is connected to the BPRN* of the next higher priority master and so forth, and on requesting the bus, the higher priority master ripples a BPRO* to deactivate all lower priority masters.

A master can activate CBRQ* when it wants control of the Multibus interface but does not currently control it. If CBRQ* is high, it indicates that no other master is requesting the bus and therefore the present bus master, normally the CPU can retain the bus.

A5.3 BUS EXCHANGE LOGIC UNIT

The Multibus interface can accommodate several bus masters on the same system, each one taking control of the bus as it needs to affect data transfers. The bus exchange logic provides the means by which a master gains control of the bus, using the Multibus exchange signals as described in Section A5.2. The basic unit is shown in Fig. A5.2. As a master requires the bus acquisition, it asserts bus request. Flip-Flops A and B synchronize the transfer request with (BCLK*). When

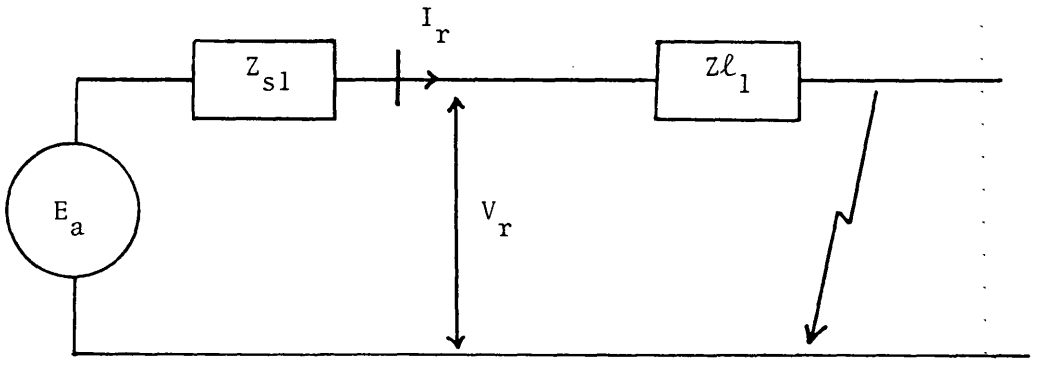


Fig. A4.1 : Equivalent circuit for three phase-earth fault network

APPENDIX 5

PROCESSOR AND MULTIPLIER UNIT TECHNICAL DESCRIPTION

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Instruction code (200)

End of file (220)

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A5.2 MULTIBUS EXCHANGE SIGNALS

The bus exchange logic unit uses a discrete logic process, prior to a DMA cycle, for the bus acquisition. To perform the required bus exchange process, five exchange signals are used, Bus Clock (BCLK*), Bus Busy (BUSY*), Bus Priority In (BPRN*), Bus Priority Out (BPRO*) and Common Bus Request (CBRQ*). Note that the (*) means active low command. The bus exchange must be synchronized with BCLK*, with the synchronization occurring with the falling edge of the 50% duty cycle pulse. The BCLK* has a frequency of 9.5 MHz.

BUSY* is a command driven by the bus master in control of the bus. When a master asserts BUSY*, the BUSY* signal prevents other bus masters from gaining control of the bus. Another master is allowed to access the bus after the bus master in control of the bus deactivates its BUSY*, to indicate the completion of its access.

The bus priority commands, BPRN* and PBRO* are used to resolve the masters priority. Active BPRN* indicates that no master of higher priority is requesting the bus. When the master request the bus it activate BPRO* to inform lower priority masters that a higher priority master bus request exists. In a serial priority scheme, the highest priority BPRO* is connected to the BPRN* of the next higher priority master and so forth, and on requesting the bus, the higher priority master ripples a BPRO* to deactivate all lower priority masters.

A master can activate CBRQ* when it wants control of the Multibus interface but does not currently control it. If CBRQ* is high, it indicates that no other master is requesting the bus and therefore the present bus master, normally the CPU can retain the bus.

A5.3 BUS EXCHANGE LOGIC UNIT

The Multibus interface can accommodate several bus masters on the same system, each one taking control of the bus as it needs to affect data transfers. The bus exchange logic provides the means by which a master gains control of the bus, using the Multibus exchange signals as described in Section A5.2. The basic unit is shown in Fig. A5.2. As a master requires the bus acquisition, it asserts bus request. Flip-Flops A and B synchronize the transfer request with (BCLK*). When

flip-flop B is set, a (CBRQ*) is activated, to indicate that a bus master is requesting the bus and (BPRO*) is activated to prevent lower priority masters from accessing the bus. As the master currently in control of the bus completes its cycle, it deactivates (BUSY*), the bus master requesting the bus becomes the bus master, by asserting the (BUSY*) command and enabling the data transfer. When the addressed slave accepts the data, it generates an acknowledge signal (XACK*), which causes the transfer request to terminate, by allowing (BUSY*) to go inactive. Fig. A5.3 shows the bus exchange logic timing diagram.

A5.4 VECTOR MULTIPLIER UNIT FUNCTIONAL DESCRIPTION

The vector multiplier unit consists of address decoders, DMA transfer parameter registers, bus exchange logic unit and a 16-bit multiplier chip. Fig. A5.4 shows the VM board block diagram.

A5.4.1 Multiplier unit address decoding

Fig. A5.5.1 shows the VM unit address decoder circuit diagram. The VM unit is memory mapped to fixed locations, $F0F0 and $00F0. The multiplicant buffer starting address vector, and the multiplicant string length are loaded through location $F0F0. The product buffer starting address vector, and the product string length are loaded through location $00F0.

The address is decoded through 16-bit digital comparators (DC1 to DC4). The comparators are enabled using the (I/O WR*) Multibus command, and the address transferred on the address bus is compared with fixed state switches. On comparing similar addresses, the digital comparator activates a status line, which latches the transferred data to its destination.

A5.4.2 DMA Parameter transfers

In order to transfer the DMA parameters, four (I/O WR*) cycles are required. The first (I/O WR*) to $FF0F transfers the multiplicant buffer starting address. The second (I/O WR*) to $00F0 transfers the products buffer starting address. The third (I/O WR*) to $FF0F latches the multiplicants buffer string length. The fourth (1/O WR*) to $00F0 latches the products buffer string length. The physical DMA transfer parameters are loaded through the 16-bit data bus. Figs. A5.5.2 and A5.6 shows the circuit diagram for the DMA parameter registers and the process timing diagram respectively.

The multiplicant buffer starting address ($9400) is loaded as a most significant byte ($94), through B2 and the least significant byte is generated using two 4-bit binary counters (C1 and C2), thus 256 source addresses can be accessed. The counters are reset to 0 when the DMA parameters are transferred. The counter outputs are incremented for each DMA transfer.

The source word counter is latched to two programmable up/down counters (C3 and C4). The source word counters are loaded to the counter data lines, which sets the (BORROW*) line inactive. The counters are decremented for each data transfer (using count down mode). When the counters reach 0, the (BORROW*) line goes active, which indicates that the source string data transfers are completed. Thus, the DMA read channel is disabled. Similarly, the destination (products) buffer starting address ($9800), and the destination string length is transferred using the technique described above. Fig. A5.5.3 shows the circuit diagram for the destination parameter transfers.

The following procedure is used to program the VM unit DMA transfer parameters:

1 - Load the source buffer starting address ($9400), by performing (I/O WR*) to ($F0F0).

2 - Load the destination buffer starting address ($9800), by performing (I/O WR*) to ($00F0).

3 - Latch the multiplicant string length, by performing (I/O WR*) to ($F0F0).

4 - Latch the products string length, by performing (I/O WR*) to ($00F0).

Following the latching of the products string length, the DMA unit is activated. With respect to the DMA parameter programming, it must be noted that the unit is accessed as a slave, thus a (XACK*) signal is generated, 400 ns following the data transfers of steps 1 to 4. The DMA unit is enabled as a bus master.

A5.4.3 VM Unit bus exchange logic

The VM bus exchange logic unit is a modification of the basic bus exchange logic described in Section A5.3. Figs. A5.5.4 and A5.5.5 show the VM exchange logic circuit diagram. When the VM unit requests a DMA transfer cycle, the bus exchange logic unit asserts the required handshake signals for the bus control, as described in Section A5.3. The memory read/write commands are controlled by the two least significant bits of a binary counter (C5 in Fig. A5.5.5). The counter two least significant bits status are shown in Table A5.1.

Qb	Qa
0	0
0	0
0	0
0	0
1	0
0	0
0	0
1	0
=	=
0	0
0	0
1	0
1	0

Table A5.1 : Rd/WR channels control

With respect to Table 5.1, it must be noted that Qb = 0 represents a multiplicant read and Qb = 1 represents a product write cycle. The technical detail of Table A5.1 will be discussed in Section A5.4.4.

A5.4.4 Multiplier chip

Fig. A5.5.6 shows the multiplier chip circuit diagram. The multiplier input registers are positive edge triggered. The input clock signals (CLKX and CLKY) are generated through a flip-flop (D4). As the DMA unit performs a read cycle, the processor unit RAM places the multiplicant data on the Multibus output buffer and generates a transfer acknowledge signal, which initiates a multiplier input register clock. The product becomes available 100 ns following the latching of the Y multiplicant. However, the multiplier chip is not provided with a

status line to indicate the multiplication cycle and the multiply time is a function of the chip temperature. In order to ensure that the multiply cycle is completed, the products are clocked out after 250 ns (150 ns for maximum multiplication time and 100 ns safety margin). In order to avoid the 250 ns wait state, the multiplication can be realized such that as the multiplier performs one multiplication, the product of the previous multiplication is retrieved. The process timing diagram is shown in Fig. A5.7. As shown in Fig. A5.7, when X1 and Y1 are clocked to their corresponding registers, the read write control counter, described in Section A5.4.3, is prevented from initiating a write cycle by resetting the counter. Following the resetting of the counter, two read cycles are initiated, to latch X2 and Y2. As Y2 is clocked to its register, a CLKM signal is initiated to clock P1 from the product register.

As the multiplicant string counter reaches zero, the counter (BORROW1*), see Section A5.4.2, initiates an additional write cycle to transfer the last product. With respect to the product transfer, it must be noted that the multiplier chip is used in single precision mode (only the most significant 16-bits are retrieved).

The multiplier chip data registers are provided with internal tri-state buffers, thus the multiplicant data can use a common data bus. The multiplicant data is transferred to or from the processor data through two 16-bit data transceivers (T1 and T2). The transceivers are enabled by the DMA unit. The data flow direction is controlled by the product address enable (AENWR*). When (AENWR*) is active, the transfer data flow is from B to A, otherwise data flow is from A to B (read cycle).

A5.5 STC CLOCK SOURCE AND SUB-SCALERS

The STC is provided with on-chip 2.45 MHz oscillator. A 16-bit scaling counter, tapped every 4-bits, divides the output into four additional sub-frequencies, as shown in Fig. A5.8. This provides a total of 5 internal frequencies that can be routed to any of the five general purpose counters. For the generation of the relay timing signals, the oscillator output is directly scaled to generate the required timing signals.

A5.5.1 Counter logic group (CLG)

The STC is provided with five counter logic groups. Each counter consists of a 16-bit general purpose counter, with associated control, data pointer counter and command mode registers. The control register determines the specific operation of each counter.

A5.5.1.1 Data pointer counter

The 6-bit data pointer, Fig. A5.9, is used to control the internal addressing of the CLG. The data pointer is memory mapped as $FFD2, and can be accessed by the host CPU through I/O commands. The data pointer is used to initialize a specific CLG and load the scaling factor for the counter operation.

A5.5.1.2 Counter mode register (CM)

Each CLG includes a CM register, used to control the individual operation of the counter. The 16-bit CM register bit assignment is shown in Fig. A5.10. With respect to Fig. A5.10, it must be noted that the least significant byte (CM0 - CM7) is loaded with $22, for all counter operations required for the relay timing signals. The most significant

byte (CM8 - CM15) is specified for each counter operation according to Table A5.2:

CLG	CM8 - CM15($)	Description
1	1B	F1 is the clock source for CLG1
2	12	CLG1 output is the clock source for CLG2
3	13	CLG2 output is the clock source for CLG3
4	04	CLG3 output is the clock source for CLG4
5	05	CLG4 output is the clock source for CLG5

Table A5.2 : CM register most significant byte assignment

The technique described in Table A5.2, by using the output of each CLG as a source input to the next CLG produces synchronous timing waveforms, as required by the relay.

A5.5.2 STC Programming procedure

The following procedure is used to program the STC:

1 - Enter Master reset STC command, by writing $FFFF to the STC control port ($FFD0).

2 - Enter command to switch to 16-bit data bus operation, by writing $FFEF to the STC control port ($FFD0).

3 - Enter command to initialize the data pointer for the first CLG, by writing $FF01 to the STC data port ($FFD2). The E fields in Fig. A5.9 must be filed with zeros.

4 - Load CM, to specify the initialized CLG operation, using the format

described in Section A5.5.1.2, by writing a 16-bit word to the STC control port ($FFD0).

5 - Enter command to load the data pointer, by writing $FF09 to the STC data port. The E field in Fig. A5.9 must be 01.

6 - Load scaling factor to CLG1, by writing to the STC control port ($FFD0). In this respect it must be noted that the output control circuitry for each CLG includes a toggle flip-flop that generates an output waveform at half frequency specified by the scaling factor.

7 - Repeat steps 3, 4, 5 and 6 for all CLGs to be programmed.

8 - Load and Arm selected counters, by writing an STC command to the command port ($FFD0). The load and arm command format is shown in Fig. A5.11. With respect to Fig. A5.11, the selected combination of counters, as specified in the S field will be loaded by the previously entered value. CLG counters must be armed before counting can commence.

9 - Enable counter outputs by writing an STC command to the control port ($FFD0). The enable output command format is shown in Fig. A5.12. The armed counter outputs toggle for counter N if enabled.

A5.5.3 STC Status register

The 8-bit read-only register indicates the state of the output signal for each of the general purpose registers. The bit assignment of the status register is shown in Fig. A5.13. The output signals reported are those before the interface buffer circuitry. Thus, the status register reflects the polarity of the output signals. The status register is accessed by reading the STC control port ($FFD0).

A5.6 D/A CONVERTER UNIT TECHNICAL DESCRIPTION

Fig. A5.14 shows the D/A converter circuit diagram. The D/A is memory mapped as location $5005. The address is decoded through an 8-bit digital comparator, which compares the 4 least and most significant bits ($55) with a fixed state input. On comparing similar addresses, the digital comparator status latches the data to two sets of octal flip-flops. The digital data which appears on the flip-flops outputs is converted to an analogue signal. The D/A unit is accessed as a bus slave, and an (XACK*) signal is generated 400 ns following each access.

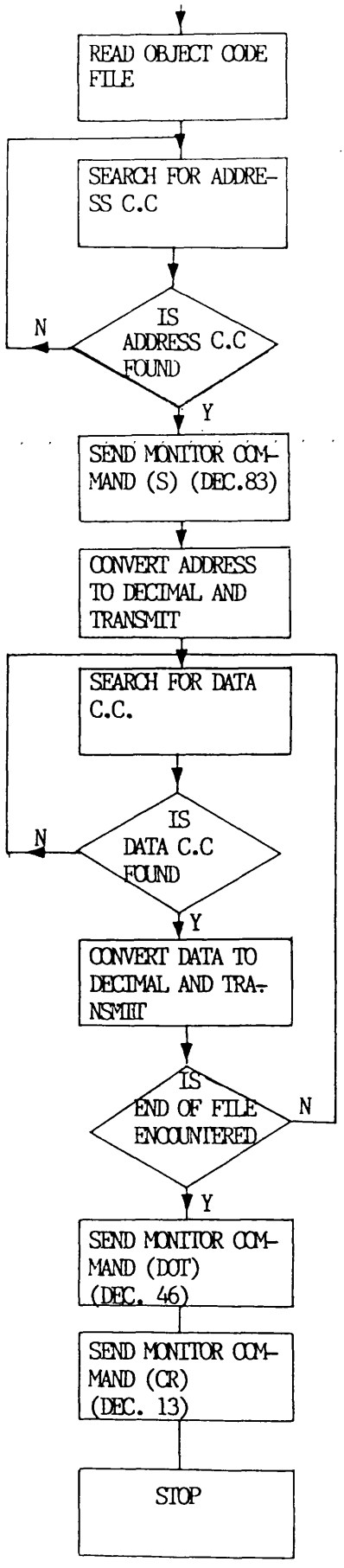


Fig. A5.1 : Z8002 download program flow chart

note: Address control code (C.C.) = (Octal 204)
Data " " = (Octal 200)
End of file " " = (Octal 220)

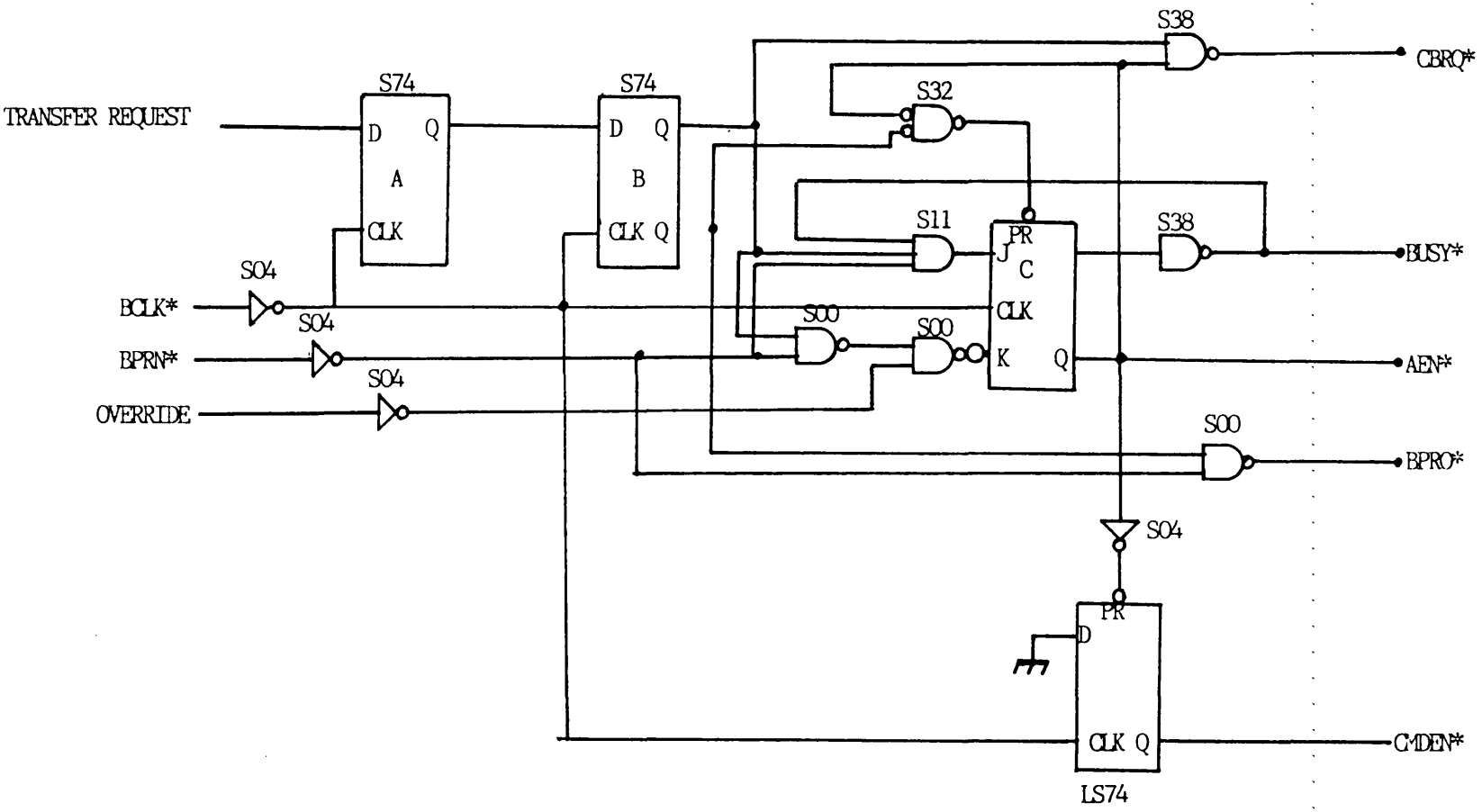


Fig. A5.2 : Bus exchange logic basic unit

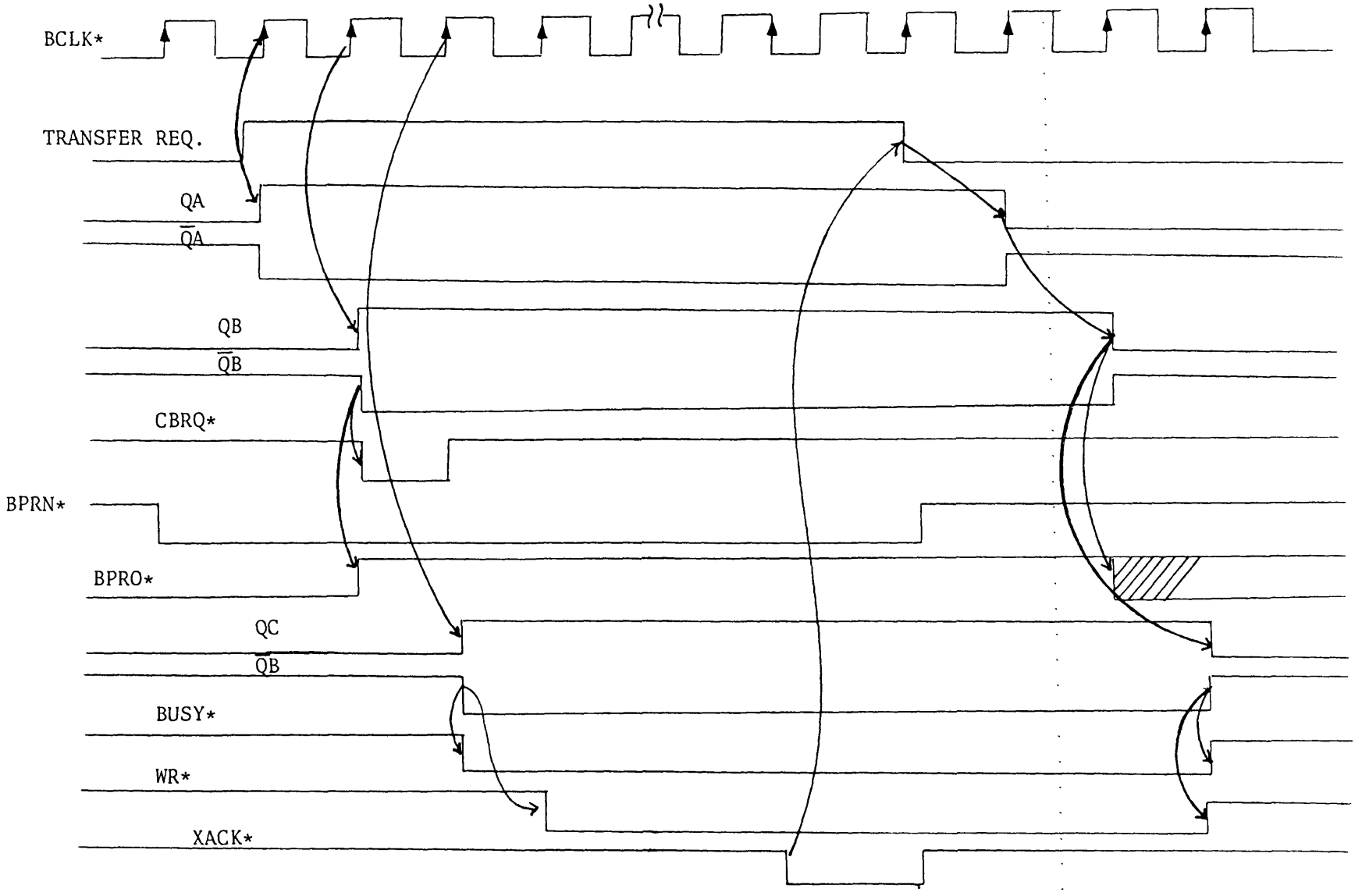


Fig. A5.3 : Bus Exchange Timing Diagram

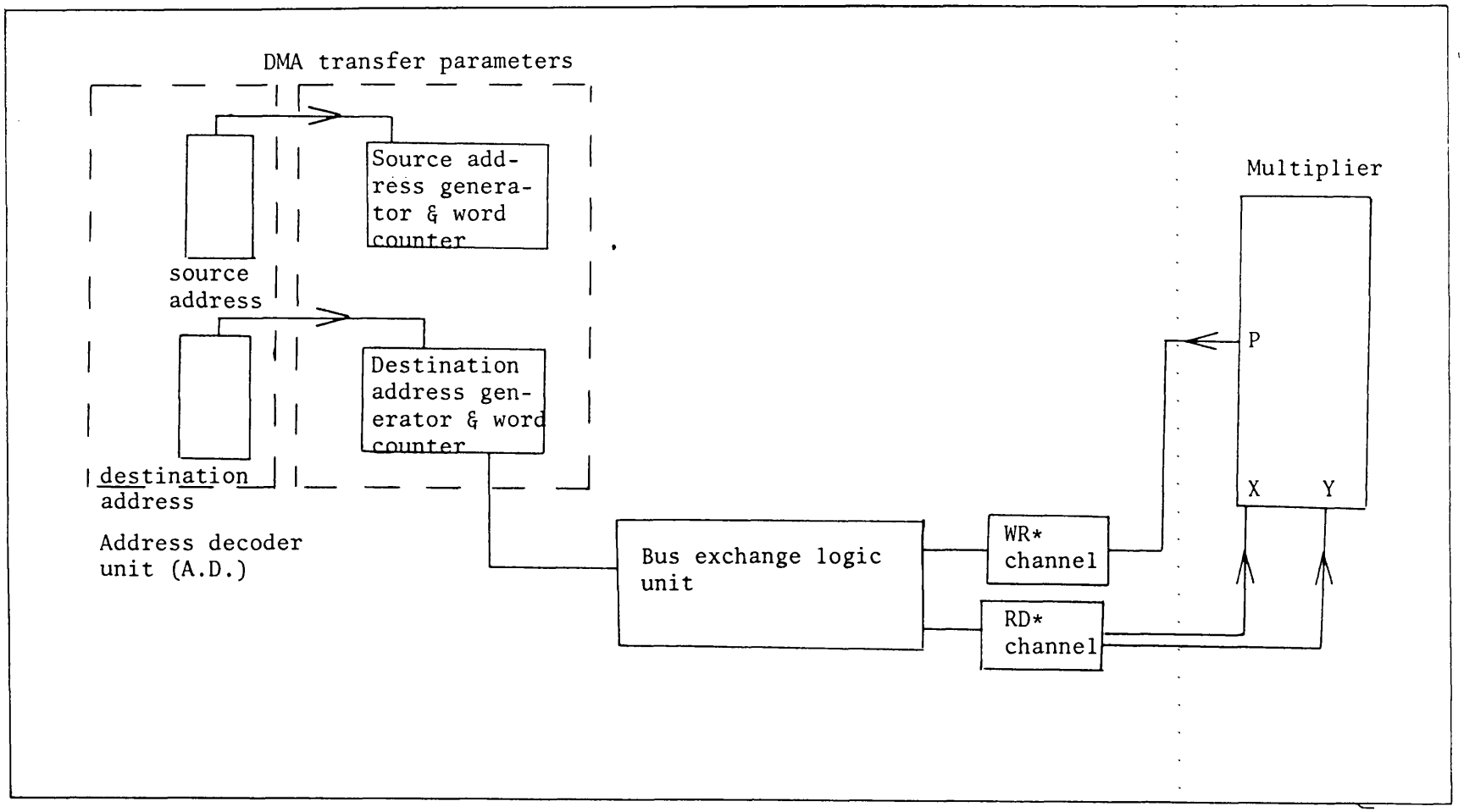


Fig. A5.4 : Vector multiplier board block diagram

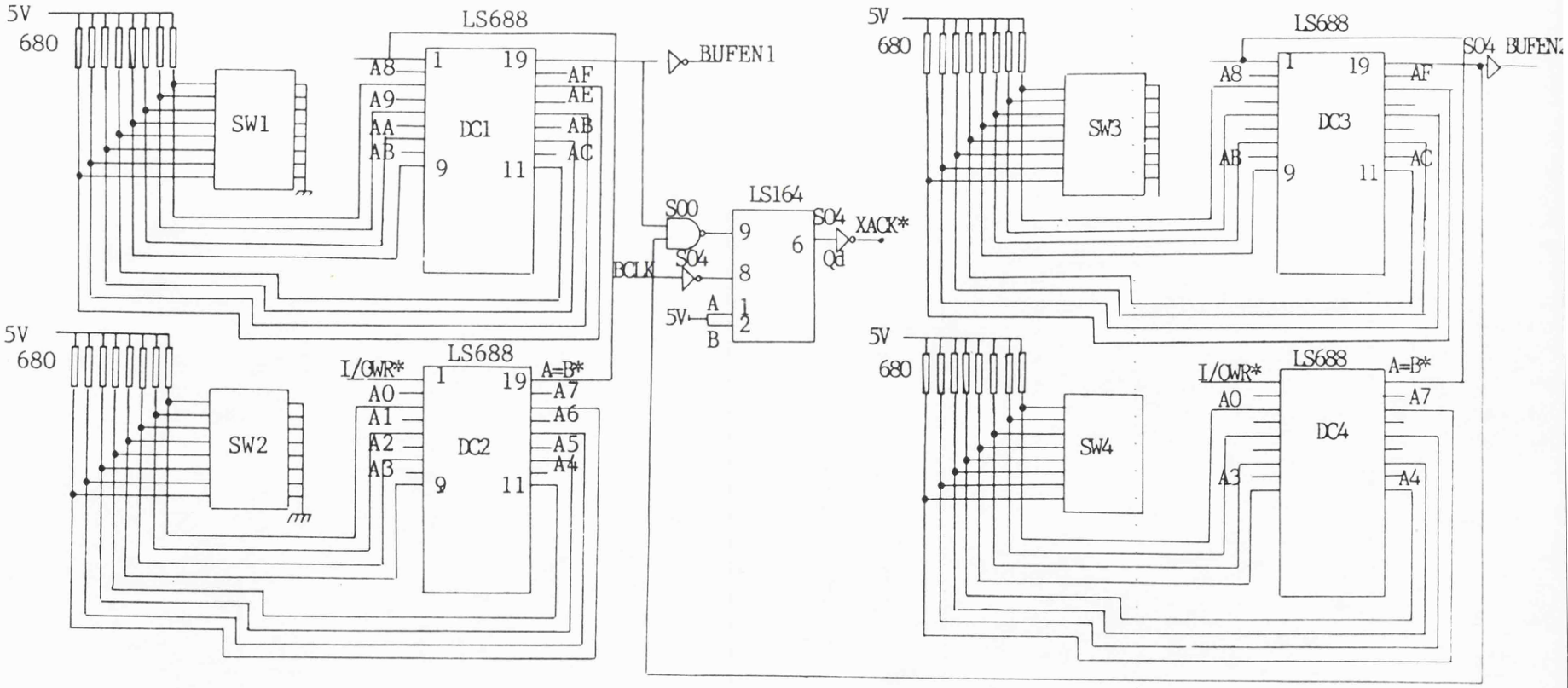


Fig. A5.5.1 : VM board address decoder unit

All resistors are in Ω unless otherwise specified
All capacitors are in μF unless otherwise specifie

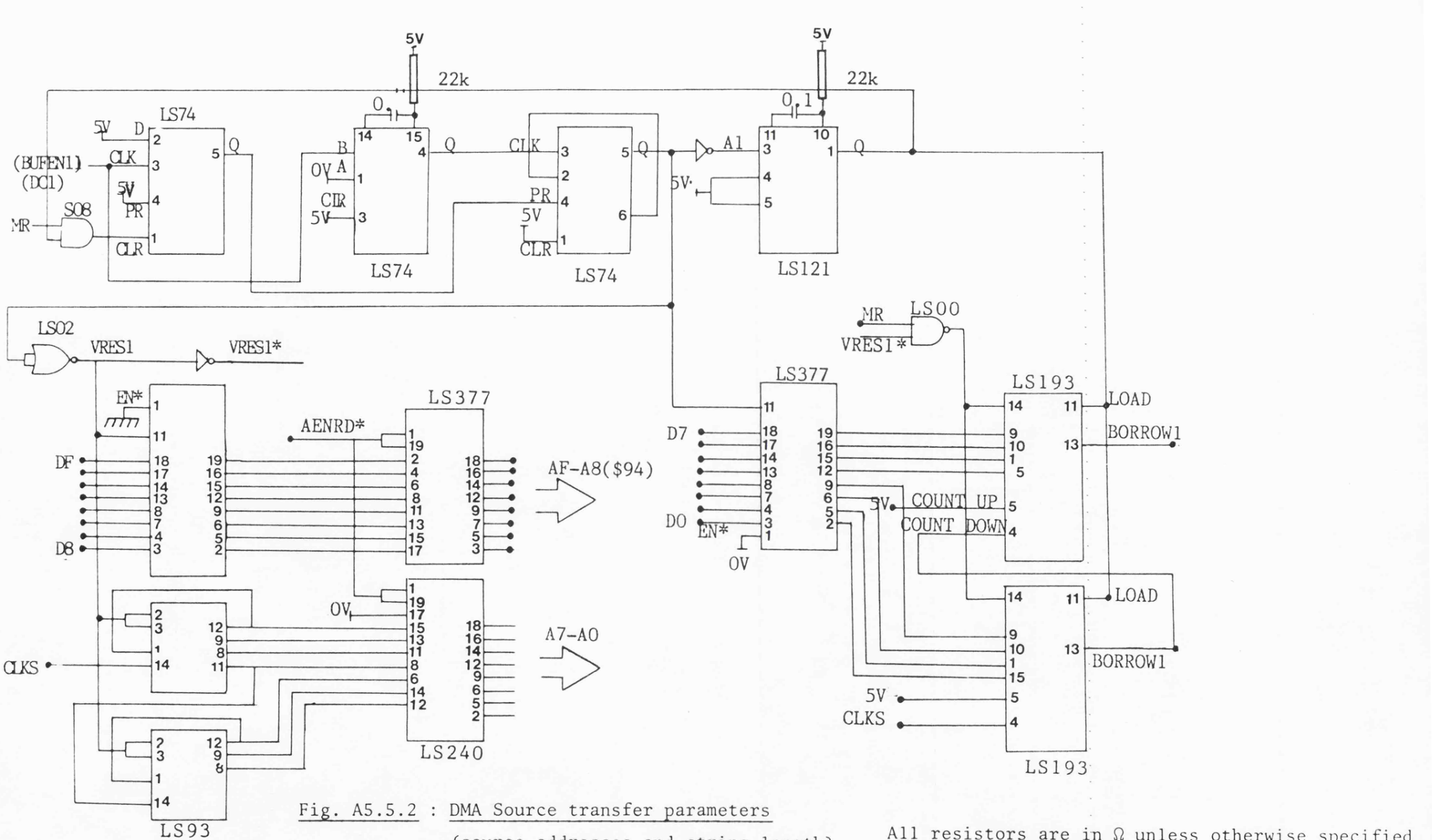


Fig. A5.5.2 : DMA Source transfer parameters (source addresses and string length) circuit diagram

All resistors are in Ω unless otherwise specified
All capacitors are in μF unless otherwise specified

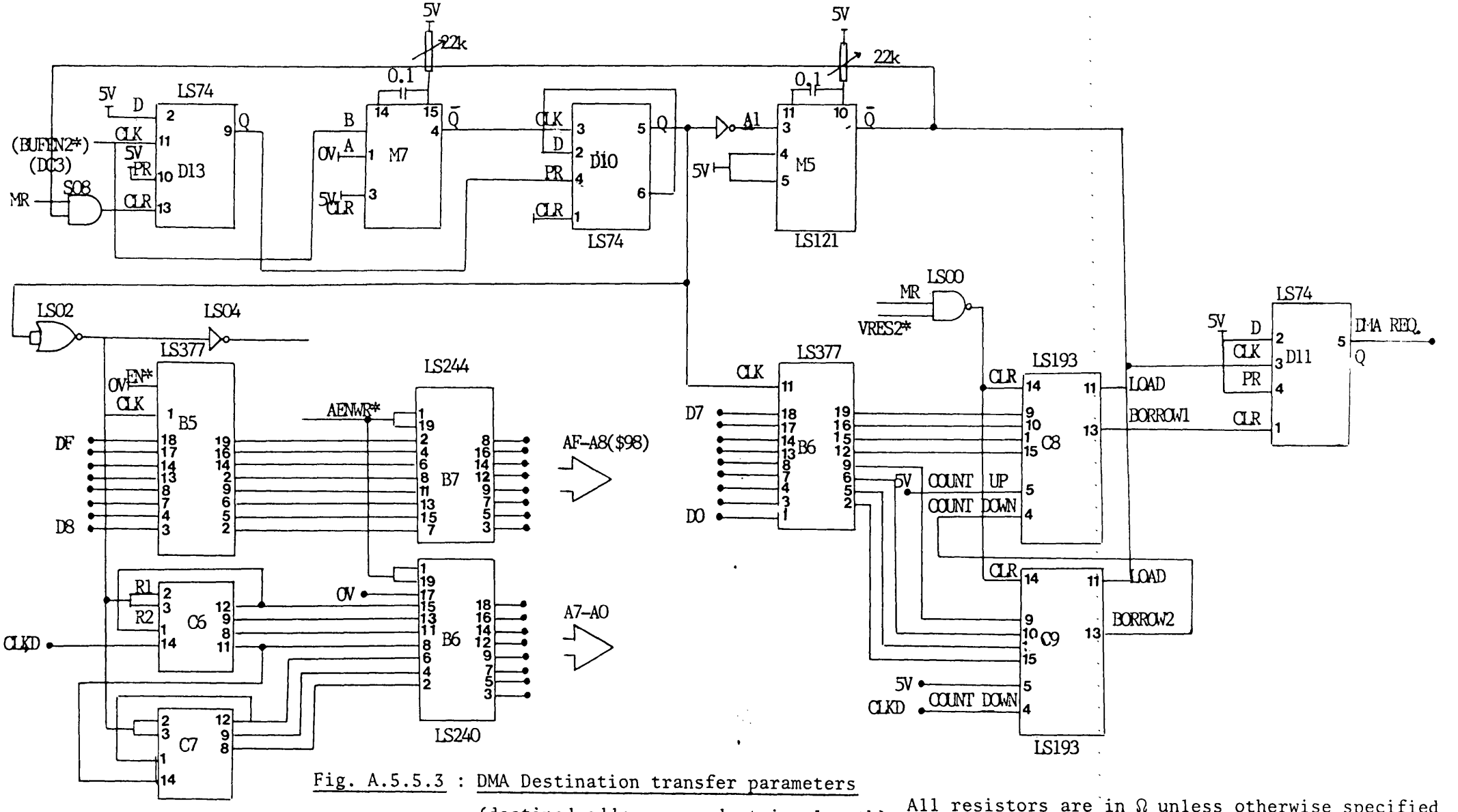


Fig. A.5.5.3 : DMA Destination transfer parameters (destined addresses and string length) circuit diagram

All resistors are in Ω unless otherwise specified
All capacitors are in μF unless otherwise specified

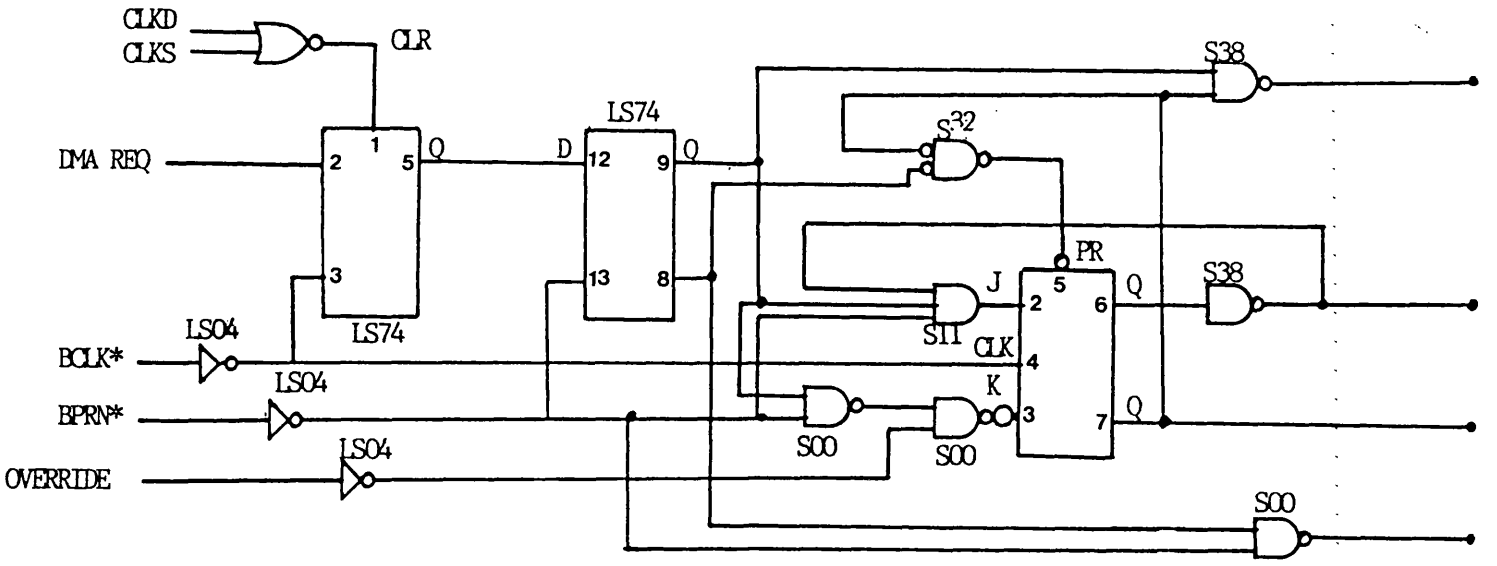


Fig. A5.5.4 : VM unit bus exchange logic circuit diagram

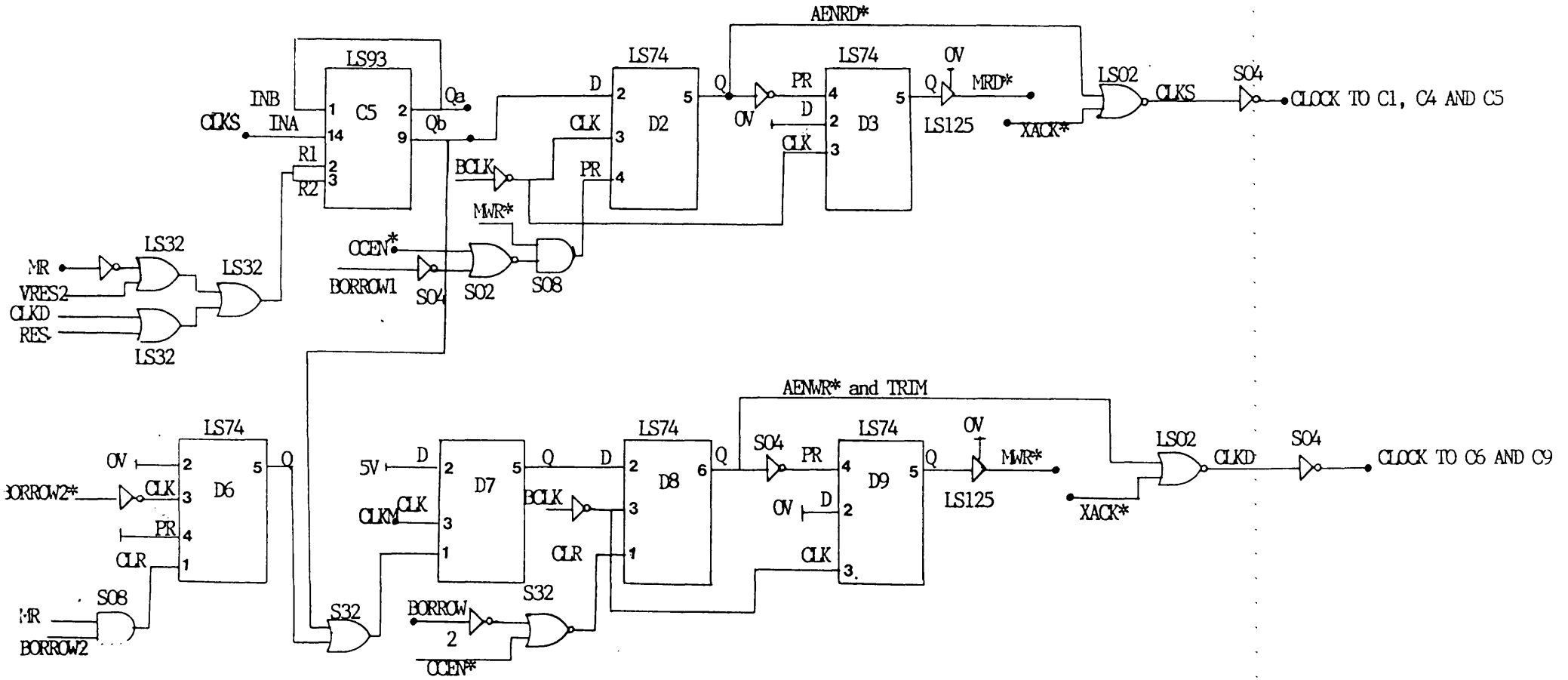


Fig. A5.5.5 : VM unit DMA read/write control channels circuit diagram

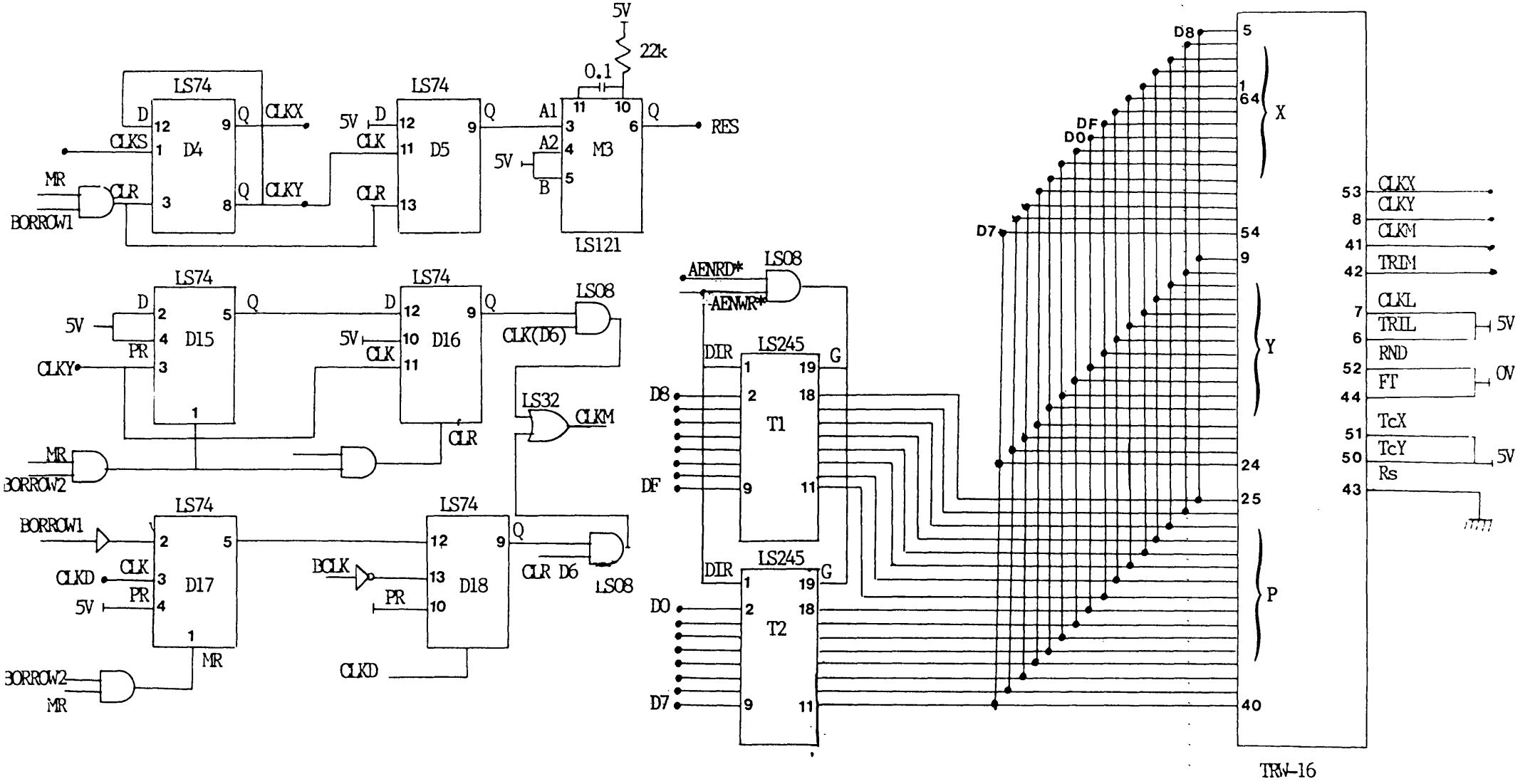


Fig. A5.5.6 : Multiplier chip control circuit diagram

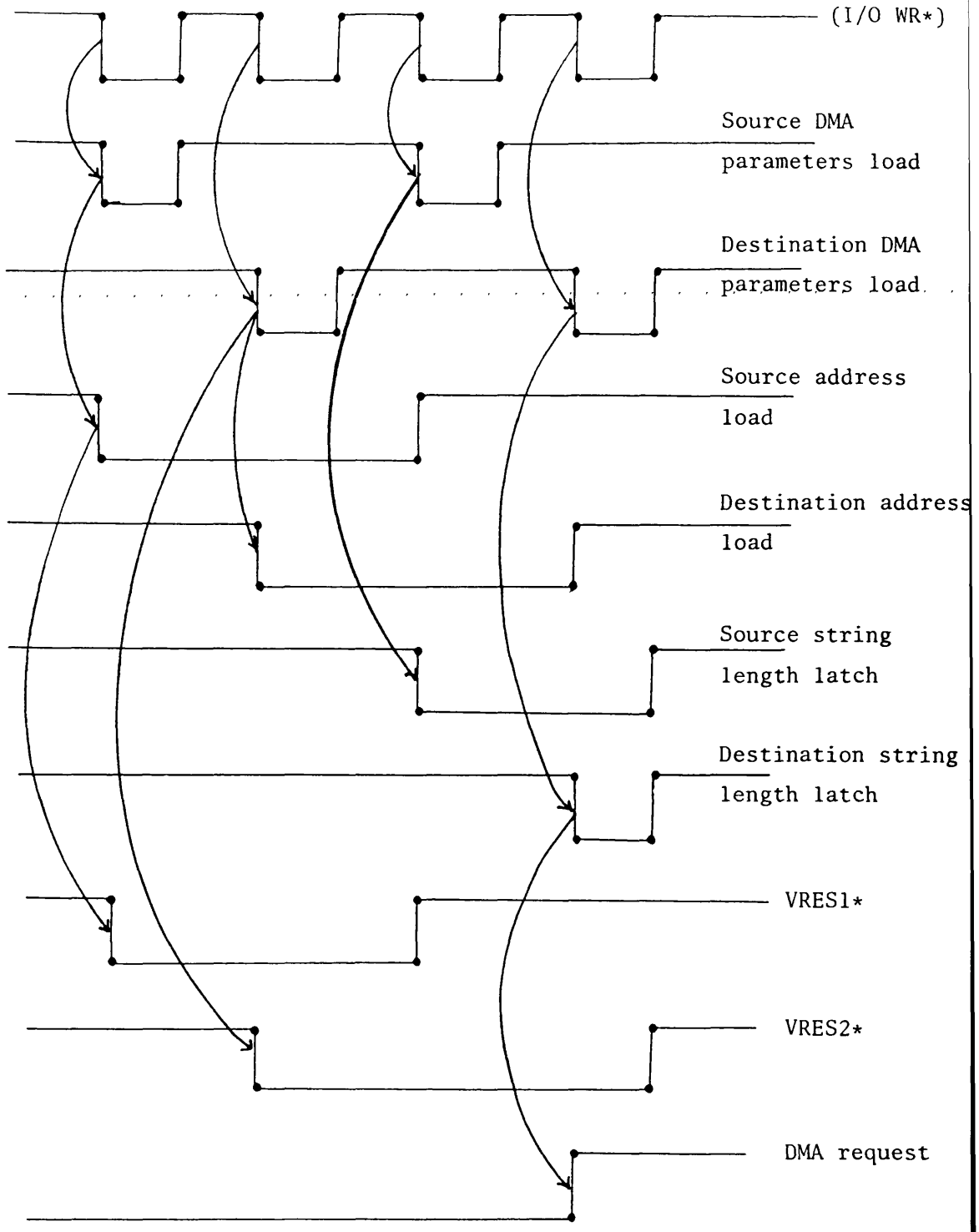


Fig. A5.6 : DMA transfer parameters timing diagram

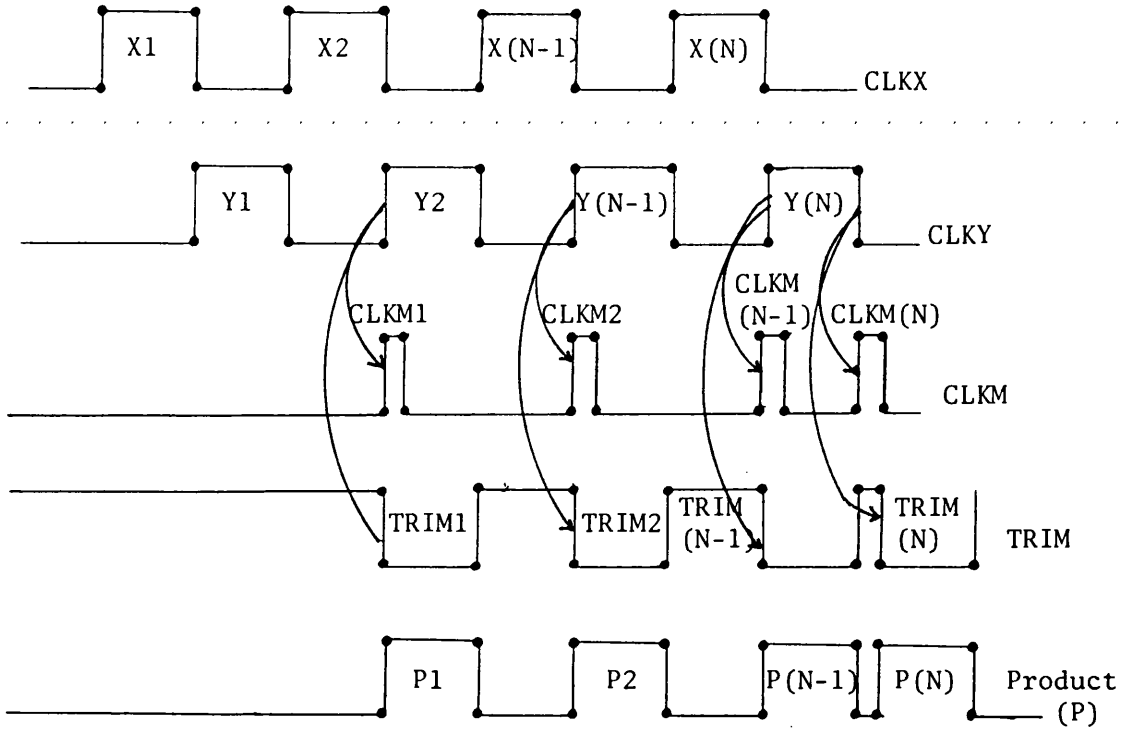


Fig. A5.7 : Multiplication process timing diagram

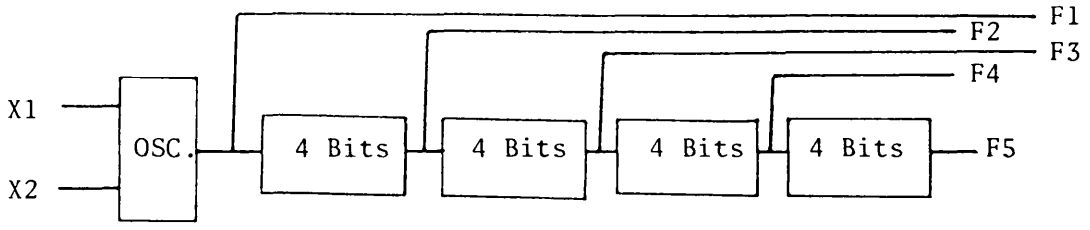
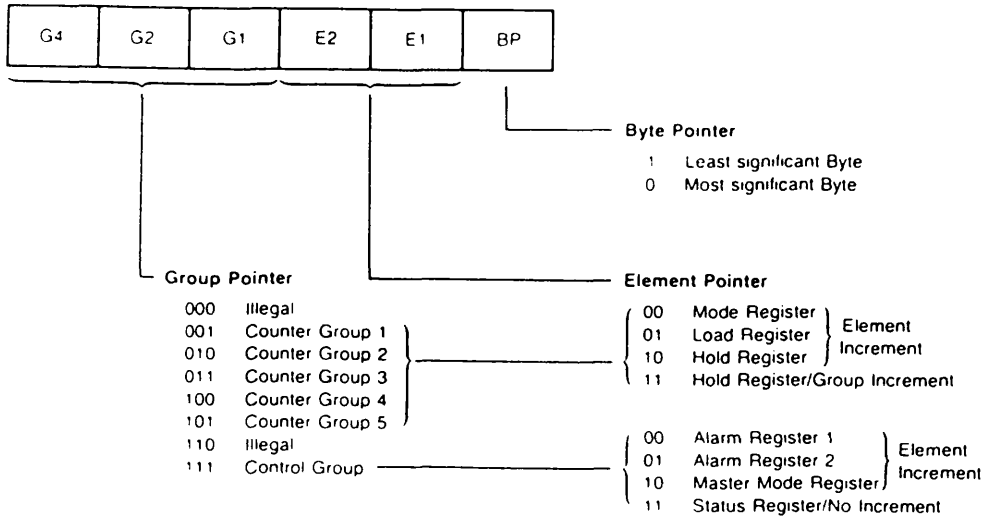


Fig. A5.8 : STC main oscillator and sub-scaler



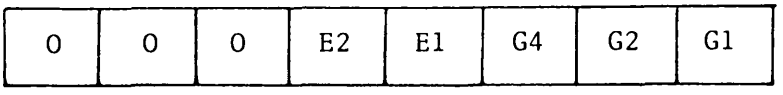


Fig. A5.9 : Data pointer register bit assignments and STC command format for the register access

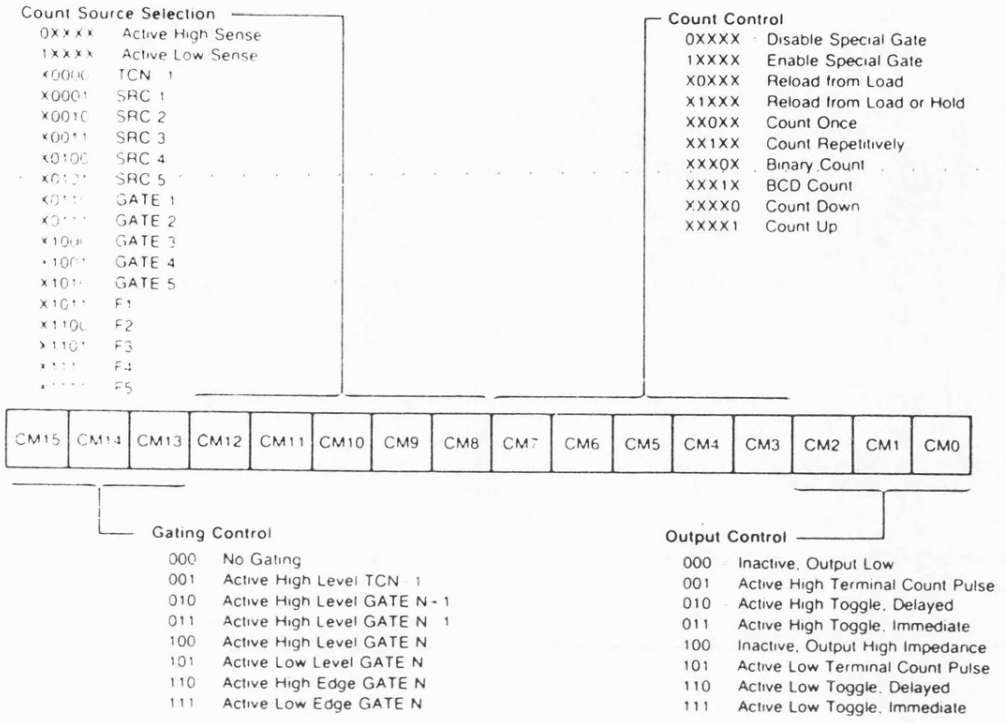


Fig. A5.10 : Counter made register bit assignments

0	1	1	S5	S4	S3	S2	S1

Fig. A5.11 : Load and arm counters STC command format

1	1	1	0	1	N4	N2	N1

Fig. A5.12 : Enable output STC command format

$001 \leqslant N \leqslant 101$

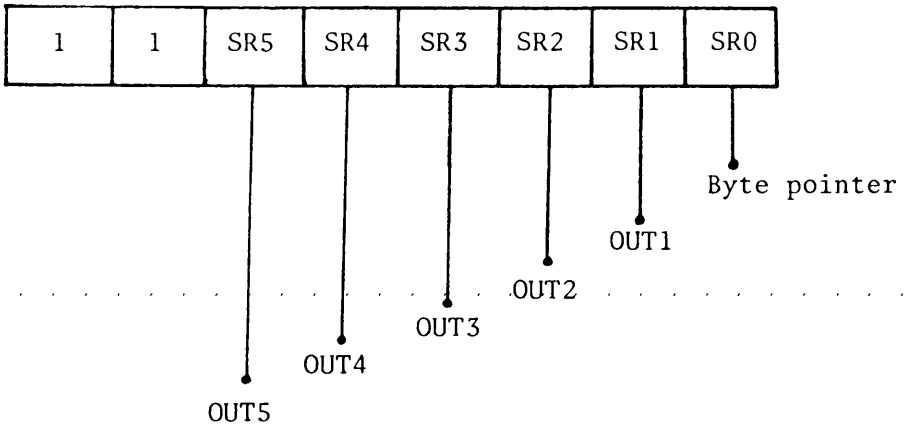


Fig. A5.13 : Status register bit assignments

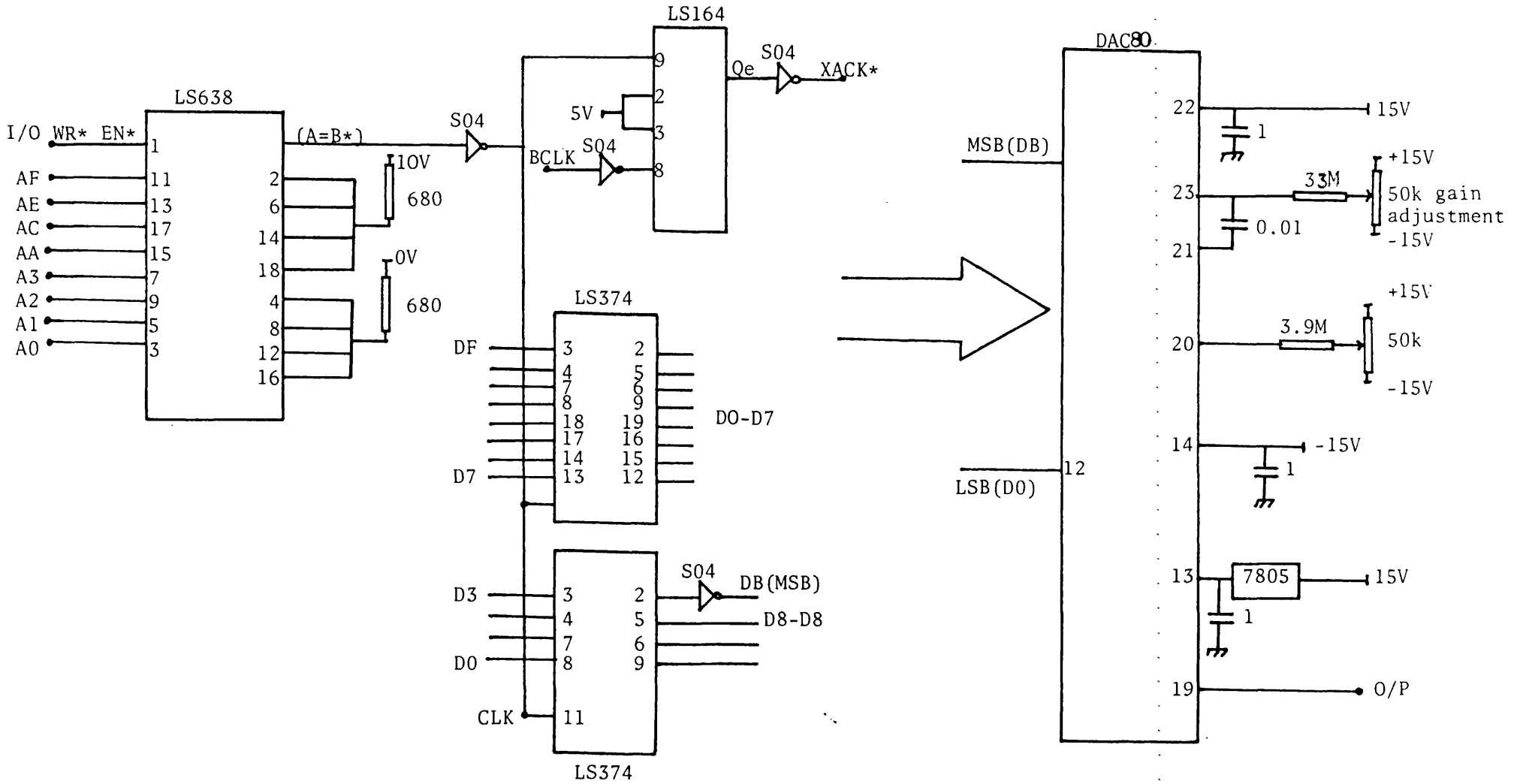


Fig. A5.14 : The D/A converter circuit diagram

All resistors are in Ω unless otherwise specified
All capacitors are in μF unless otherwise specified

APPENDIX 6

DATA ACQUISITION UNIT TECHNICAL DESCRIPTION

A6.1 TAD-32 DEVICE OPERATION

The equivalent circuit of TAD-32 is shown in Fig. A6.1. The samples are shifted through the device stages using two phase complementary square waves ϕ_1 and ϕ_2. Each new sample is introduced to the input gate with the rising edge of ϕ_1. When ϕ_1 drops, the sample value is frozen and the simultaneous rise of ϕ_2 permits the exchange of the charge stored in the input gate, which appears on the first node of the first tap. When ϕ_2 falls and ϕ_1 rises, the charge state is transferred to the second node of the tap, thus maintaining the output value for both halves of the clock period. The resulting output is designated full-wave or, full-period output, with one sample time delay between the samples as they appear at successive output taps. Fig. A6.2 shows the device operation timing diagram. In order to realize the required filtering function, the tap outputs are multiplied by the filter coefficients, a resistor chain, and the summation of these products give the filtered version of the input signal.

A6.2 TAD-32 DRIVE CIRCUIT

The TAD-32 operation requires a two phase complementary square wave clock with 12 volt positive amplitude. The rise and fall times must be adequately short (less than 20 ns) and of minimum skew (waveforms cross at approximate 50% level). The complementary clocks ϕ_1 and ϕ_2 are provided by a CD-4013 CMOS Flip-flop, and a MPQ-2222 transistor, translates the TTL level (5 volt) square wave to CMOS level (15 volt), as required by the Flip-flop. It must be noted that the waveforms ϕ_1 and

ϕ_2 must be of equal levels, otherwise the odd-even (node 1 and node 2) output variation at each tap occurs. In order to ensure that ϕ_1 and ϕ_2 have equal level, a gain equalizer is used, so that ϕ_1 amplitude is equal to that of ϕ_2.

A6.3 MULTIPLEXER DRIVE CIRCUIT

Fig. A6.3 shows the analogue multiplexer circuit diagram. The MUX-16 output is selected from one of the 16-channels using a 4-bit binary address decoder. The discrete process solution requires uniform evaluation of measurands, thus the multiplexer is scanned at 64 kHz sampling rate. The multiplexer inputs are scanned sequentially, using a 4-bit binary counter, and each input appears on the multiplexer output for 15.6 μs, where the digital conversion and data transfers are initiated.

A6.4 A/D CONVERSION CYCLE INITIATION

Fig. A6.4 shows the A/D converter circuit diagram. A digital conversion cycle is initiated by a conversion command pulse. The 'end of conversion' status control line indicates the conversion completion. As described in Section 7.10, the A/D conversion cycles are controlled by the analogue multiplexer operation. As an input channel is selected, a start conversion is initiated 3 μs after the channel selection, to allow for the multiplexer output settling time. On conversion completion the A/D output is latched to external buffers, to await the DMA transfer cycle.

A6.5 DATA ACQUISITION DMA UNIT TECHNICAL DESCRIPTION

As described in Section 7.11, the DMA unit consists of a bus exchange logic unit (BELU) and an address generator. The BELU is based on the basic BELU described in Appendix 5. A bus exchange cycle is initiated

by the A/D conversion status line. Fig. A6.5a shows the BELU circuit diagram.

In order to utilize the transfer process efficiently, two transfer buffers, BUFA and BUFB have been used. As the DMA unit transfers the 12 transformed components for one sampling cycle to BUFA, the microcomputer manipulates the previous sampling cycle 12 transformed components, which reside in BUFB and vice-versa. Figs. A6.5b and A6.6 show the address generator circuit diagram and the address generator word format for the relaying signals memory mapping. As required by the transfer process, the address generator must be capable of generating 24 addresses. The Z8002 microcomputer board has RAM addressing space from $8000 to $FFFF, and the DMA memory address segment is chosen to start at $9000. The word transfer segment, for 24 word transfers extends from $9000 to $9016 for BUFA, and $9018 to $902E for BUFB. The transfer addresses are generated using binary counters, and to generate the required 24 addresses, a 5-bit binary counter is used. A 5-bit binary counter is capable of addressing 32 memory locations, and for practical consideration, namely less complicated logic and for further development, it has been decided to transfer the 16 multiplexer inputs, then for BUFA and BUFB, 32 memory locations are required. The 32 word transfers for memory locations $9000 to $903E, require a change in the least significant byte from $00 to $3E. The most significant byte $90 is generated using fixed state switches, as shown in Fig. A6.5b. For word transfers, the least significant bit is always 0, and bits 1 to 4 are generated using a 4-bit binary counter. On the change of bit 4 from 1 to 0, after the 16 words transferred for BUFA, a Flip-flop is set to provide the required bit 5 of the counter, which starts the 16 address access to BUFB. In order to

ensure the correct performance of the address generator, bit 5 resets at a 2 kHz rate for the 4 kHz sampling rate, thus each sampling cycle transfer starts in a defined state. The address generator operation is controlled by the bus exchange logic unit. When a DMA transfer is completed, the bus exchange logic unit initiates a pulse to advance the address counter, and thus the address of the next DMA transfer is generated.

In the event of data transfer failure, a 4-bit binary counter, with light emitter diode (LED) interface is provided, normally in the off state. If the Z8002 does not acknowledge a DMA request in 15.5 μs, the LED will be turned on. The number of LEDs turned on in every processing cycle, indicates the number of unsuccessful transfers. However, tests show that a 100% of the DMA requests are acknowledged by the Z8002, and this part of the circuit becomes redundant.

The DMA unit test shows that a transfer rate of 1 Mbyte per second is achieved, compared with 0.16 Mbyte per second for the fastest conventional transfer technique as described in Section 5.7.

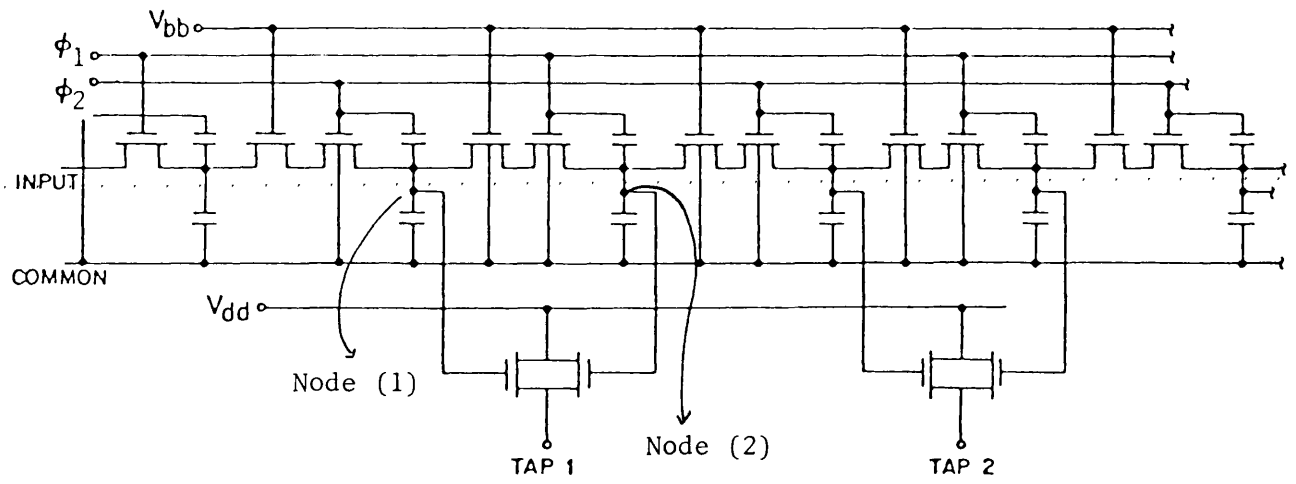
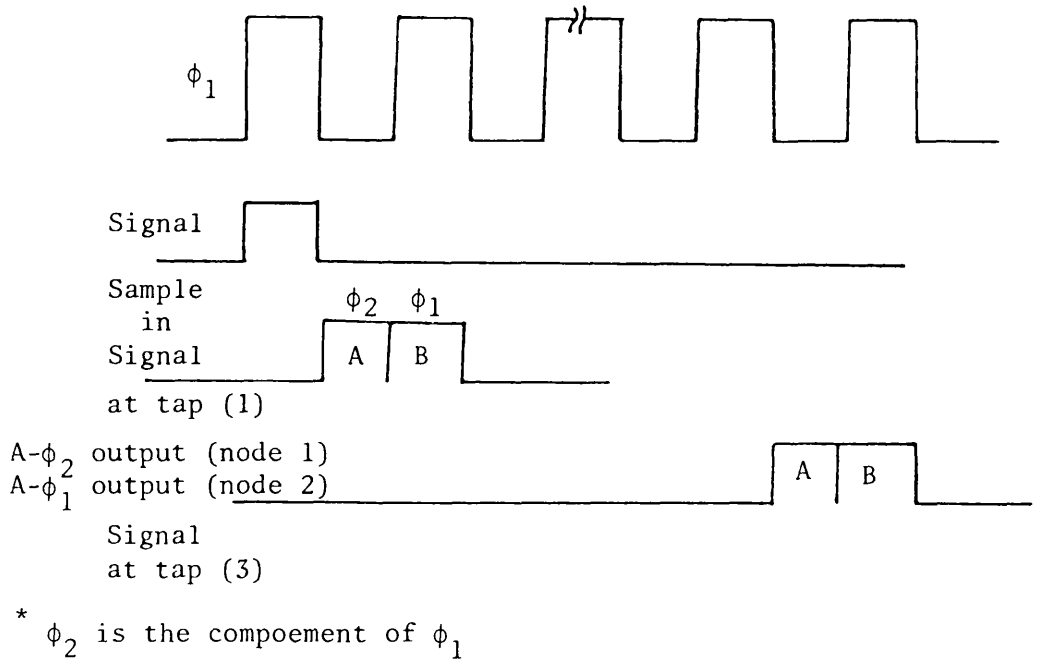


Fig. A6.1 : TAD-32 Equivalent circuit



* ϕ_2 is the compoement of ϕ_1

Fig. A6.2 : TAD-32 Operation timing diagram

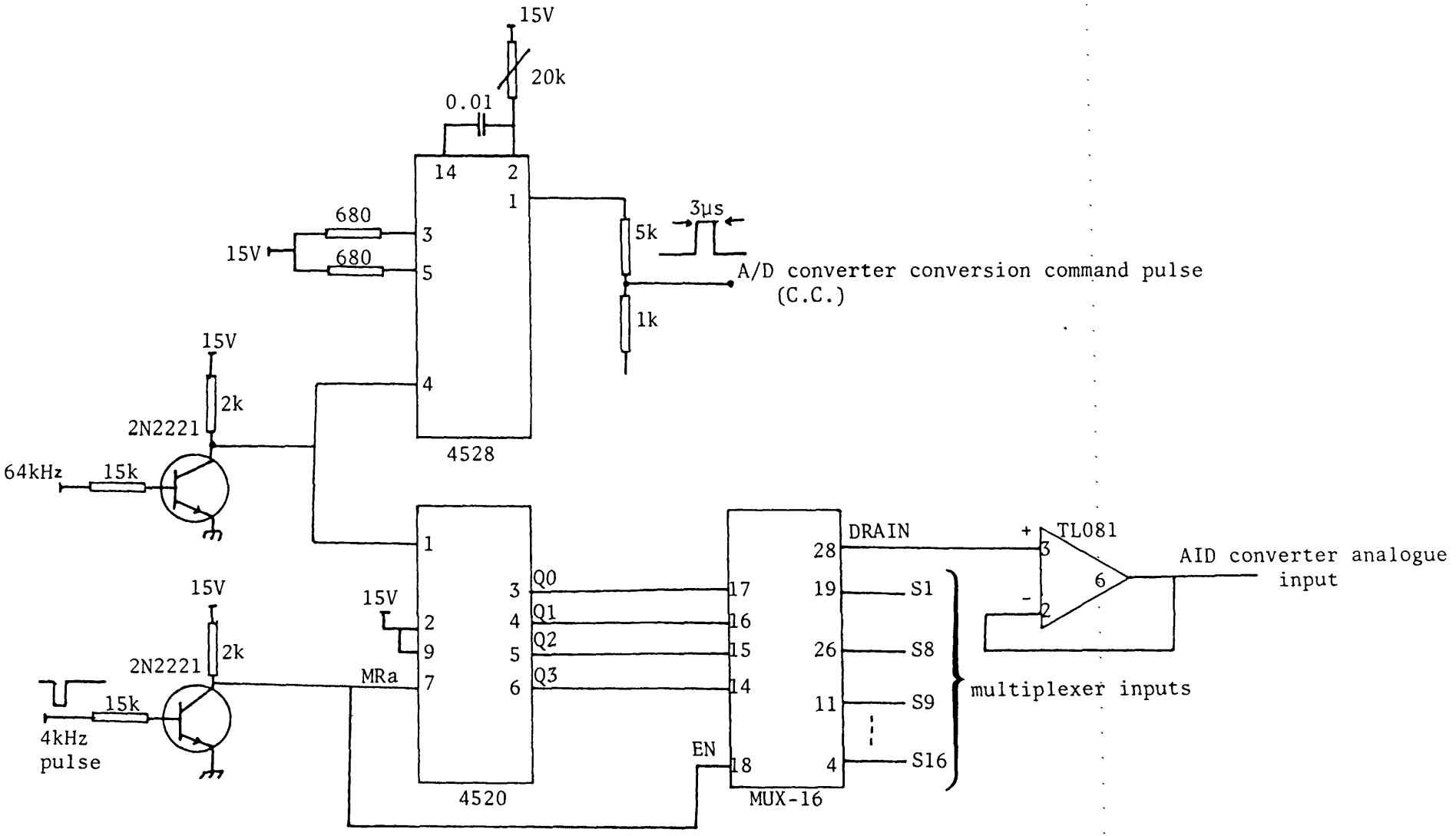


Fig. A6.3 : Analogue multiplexer circuit diagram

All resistors are in Ω unless otherwise specified
All capacitors are in µF unless otherwise specified

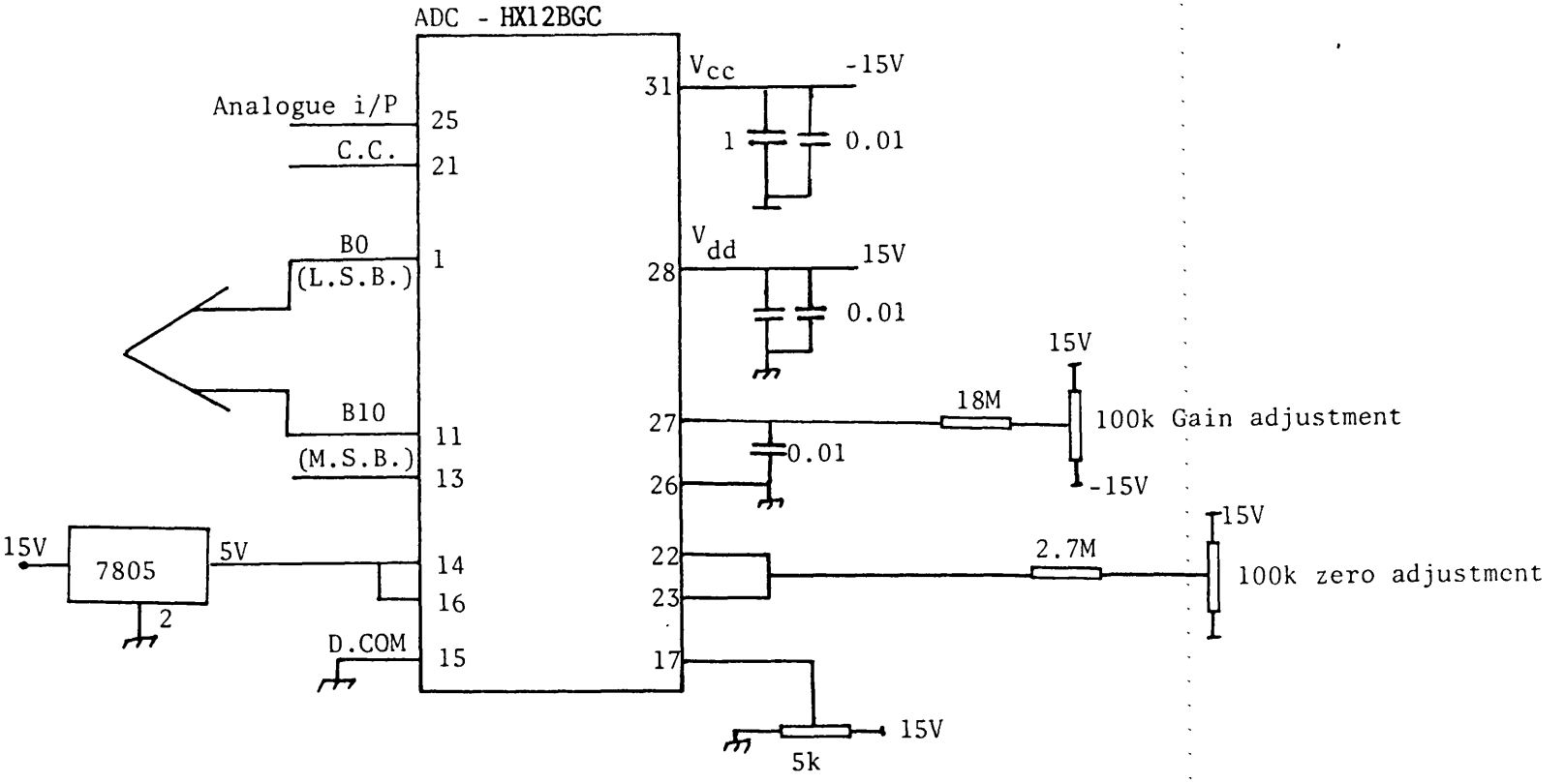


Fig. A6.4 : A/D Converter circuit diagram

All resistors are in Ω unless otherwise specified
All capacitors are in μF unless otherwise specified

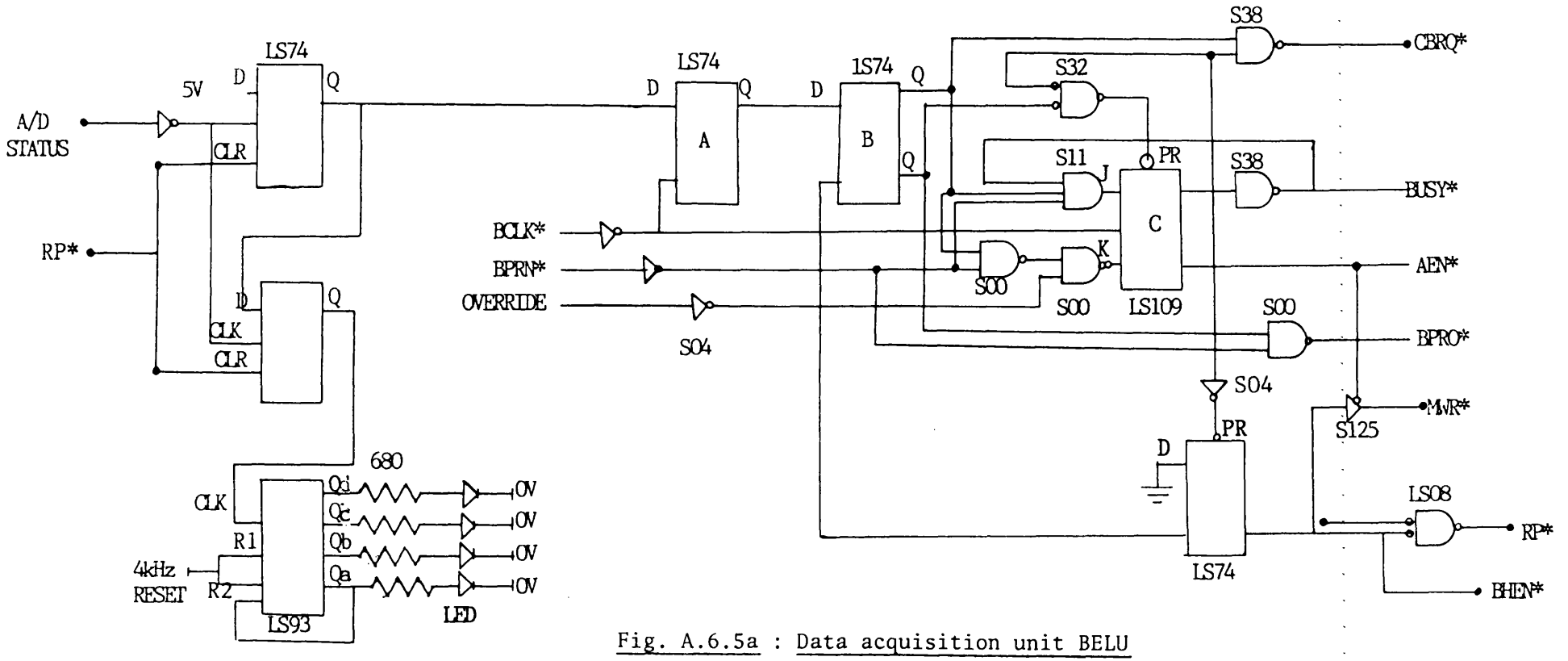


Fig. A.6.5a : Data acquisition unit BELU

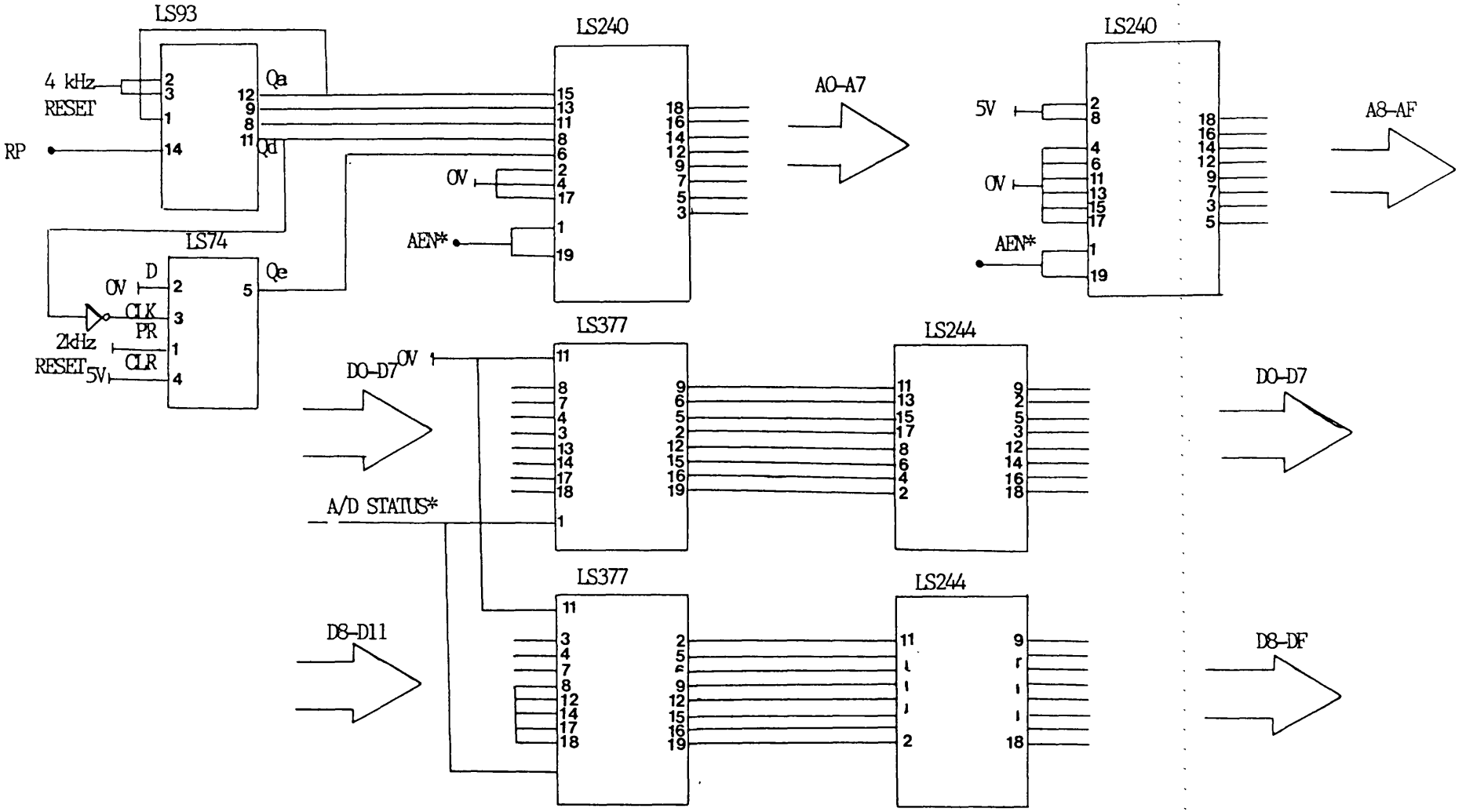


Fig. A6.5b : DAU DMA address generator unit and data buffering

A15 ---------- A0

1 0 0 1 0 0 0 0 . 0 0 E D C B A 0

MOST SIGNIFICANT BYTE

LEAST SIGNIFICANT BYTE

F.T.comp.	A7	A6	A5	A4	A3	A2	A1	A0	location(s)	BUFA
	0	0	0	0	0	0	0	0	9000	
	0	0	0	0	0	0	1	0	9002	
$i_{a1rc}(k)$	0	0	0	0	0	1	0	0	9004	
$i_{a2rc}(k)$	0	0	0	0	0	1	1	0	9006	
$v_{a1}(k)$	0	0	0	0	1	0	0	0	9008	
$v_{a2}(k)$	0	0	0	0	1	0	1	0	900A	
$i_{b1rc}(k)$	0	0	0	0	1	1	0	0	900C	
$i_{b2rc}(k)$	0	0	0	0	1	1	1	0	900E	
$v_{b1}(k)$	0	0	0	1	0	0	0	0	9010	
$v_{b2}(k)$	0	0	0	1	0	0	1	0	9012	
$i_{c1rc}(k)$	0	0	0	1	0	1	0	0	9014	
$i_{c2rc}(k)$	0	0	0	1	0	1	1	0	9016	
$v_{c1}(k)$	0	0	0	1	1	0	0	0	9018	
$v_{c2}(k)$	0	0	0	1	1	0	1	0	901A	
	0	0	0	1	1	1	0	0	901C	
	0	0	0	1	1	1	1	0	901E	
										BUFB
	0	0	1	0	0	0	0	0	9020	

SAME SEQUENCE AS BUFA

Fig. A6.6: The DMA address generator word format and signals mapping.

APPENDIX 7

EXTRACTION FREQUENCY OPTIMIZATION

For the finite Fourier Transform, the transformation window width and the extraction frequency are, in theory, arbitrary. However, the choice of the extraction frequency is governed by the behaviour of the determinant term D(t). It is desirable that D(t) has a maximum magnitude, since if it approaches zero the algorithm will become ill behaved, and noise will play a dominant role in dictating the relay operating time. As shown in this Appendix, the requirement of maximizing D(t) can be met by using an extraction frequency $f_e = 1/2T_w$.

Consider the cosine filter impulse response shown in Fig. A7.1, and let

$$h_1(\tau) = \text{COS}(\omega_e\tau + \psi_1) \qquad -T_w/2 < \tau < T_w/2 \qquad \text{--- A7.1}$$

The continuous time domain filter transfer function can be expressed in the form of Eqn. A7.2.

$$H_1(\omega_0) = \int_{-T_w/2}^{T_w/2} \text{COS}(\omega_e\tau + \psi_1)\ \text{EXP}(-j\omega_0\tau)\ d\tau \qquad \text{--- A7.2}$$

Using the identity $\text{COS}(X) = \frac{1}{2}(\text{EXP}(jX) + \text{EXP}(-jX)$ Eqn. A7.2 gives:

$$H_1(\omega_0) = \frac{\text{SIN}(\omega_e-\omega_0)}{\omega_e-\omega_0}\ \text{EXP}(j\psi_1) + \frac{\text{SIN}(\omega_e+\omega_0)}{\omega_e-\omega_0}\ \text{EXP}(-j\psi_1) \qquad \text{--- A7.3}$$

Eqn. A7.3 can be expressed in the form of Eqn. A7.4:

$$H_1(\omega_0) = B\ \text{EXP}(j\psi_1) + A\ \text{EXP}(-j\psi_1) \qquad \text{--- A7.4}$$

where

$$A = \frac{SIN(\omega_e - \omega_0)}{\omega_e - \omega_0} \qquad \text{--- A7.5}$$

$$B = \frac{SIN(\omega_e + \omega_0)}{\omega_e + \omega_0} \qquad \text{--- A7.6}$$

Similarly, the sine filter transfer function $H_2(\omega_0)$ can be expressed in the form of Eqn. A7.7.

$$H_2(\omega_0) = B\ EXP(j\psi_2) + A\ EXP(-j\psi_2) \qquad \text{--- A7.7}$$

Applying the shift theorem in the form of Eqn. A7.8,

$$\{h_1(\tau - T_w/2)\} = \{h_1(\tau)\}\ EXP(-j\omega_0 T_w/2) \qquad \text{--- A7.8}$$

The causal transfer functions of the filter, i.e. $0 < \tau < T_w$, may be written as follows:

$$H_1(\omega_0) = \left(B\ EXP(j\psi_1) + A\ EXP(-j\psi_1)\right) EXP(-j\omega_0 T_w/2) \qquad \text{--- A7.9}$$

$$H_2(\omega_0) = \left(B\ EXP(j\psi_2) + A\ EXP(-j\psi_2)\right) EXP(-j\omega_0 T_w/2) \qquad \text{--- A7.10}$$

If the filter parameters are chosen such that:

$$\psi_2 = \psi_1 + \pi/2 \qquad \text{--- A7.11}$$

then, using the identity $EXP(jX) = COS(X) + j\ SIN(X)$, Eqn. A7.10 can be expressed as follows.

$$H_2(\omega_0) = \left(jB\ EXP(j\psi_1) - jA\ EXP(-j\psi_1)\right) EXP(-j\omega_0 T_w/2) \qquad \text{--- A7.12}$$

As shown in Section A7.1, the determinant term is independent of the filter parameter (ψ_1), hence Eqns. A7.9 and A7.12 can be simplified by letting $\psi_1 = 0$.

$$H_1(\omega_0) = (B + A)\ EXP(-j\omega_0 T_w/2) \qquad \text{--- A7.13}$$

$$H_2(\omega_0) = j(B - A)\ EXP(-j\omega_0 T_w/2) \quad \text{--- A7.14}$$

As shown in Appendix 3, the determinant term D(t) can be expressed as:

$$D(t) = |H_1(\omega_0)|\ |H_2(\omega_0)|\ I_p^2\ SIN(\phi_{11}-\phi_{12})\ SIN(\omega_0 T_s) \quad \text{--- A7.15}$$

Eqn. A7.15 can be written as:

$$D(t) = I_p^2\ Im\ \{H_1(\omega_0)\ H_2^*(\omega_0)\}\ SIN(\omega_0 T_s) \quad \text{--- A7.16}$$

where Im is the imaginary component and $H_2^*(\omega_0)$ is the complex conjucate of $H_2(\omega_0)$. Substituting Eqns. A7.13 and A7.14 to Eqn. A7.16 gives:

$$D(t) = I_p^2\ Im\ \{-j(B+A)(B-A)\}\ SIN(\omega_0 T_s) \quad \text{--- A7.17}$$

Eqn. A7.17 can be expressed as:

$$D(t) = I_p^2\ (A^2 - B^2)\ SIN(\omega_0 T_s) \quad \text{--- A7.18}$$

which shows that D(t) magnitude is dictated by the term $(A^2 - B^2)$. Fig. A7.2 shows the term $(A^2 - B^2)$ for various transformation windows against the extraction frequency, and clearly shows that the maximum magnitude of $(A^2 - B^2)$ is at a frequency of about $1/2T_w$ for a given transformation window T_w.

A7.1 D(k) FINITE TRANSFORM ANALYSIS

Consider the determinant term, which can be expressed by Eqn. 4.24 as follows.

$$D(k) = i_1(k-1)\ i_2(k) - i_1(k)\ i_2(k-1) \quad \text{--- A7.19}$$

Eqn. A7.19 can be expressed as follows.

$$D(k) = \text{Im}\ \{i(k)\ i^{*}(k-1)\} \qquad \text{--- A7.20}$$

where the complex terms i(k) and i(k-1) are defined by Eqns. A7.21 and A7.22.

$$i(k) = i_1(k) + j\ i_2(k) \qquad \text{--- A7.21}$$

$$i(k-1) = i_1(k-1) + j\ i_2(k-1) \qquad \text{--- A7.22}$$

Consider a pure sinusoidal input, $i(t) = I_p\ \text{COS}(\omega_0 t + \theta)$, then $i_1(t)$ can be expressed as follows.

$$i_1(t) = \frac{I_p}{2}\ [H_1(\omega_0)\ \text{EXPj}(\omega_0 t + \theta) + H_1^{*}(\omega_0)\ \text{EXP-j}(\omega_0 t + \theta)] \qquad \text{--- A7.23}$$

Eqn. A7.23 can be expressed in the discrete domain, where $t = kT_s$ as follows.

$$i_1(k) = \frac{I_p}{2}\ [H_1(\omega_0)\ \text{EXPj}(\omega_0 kT_s + \theta) + H_1^{*}(\omega_0)\ \text{EXP-j}(\omega_0 kT_s + \theta)] \qquad \text{--- A7.24}$$

Similarly, $i_2(k)$ can be expressed as follows.

$$i_2(k) = \frac{I_p}{2}\ [H_2(\omega_0)\ \text{EXPj}(\omega_0 kT_s + \theta) + H_2^{*}(\omega_0)\ \text{EXP-k}(\omega_0 kT_s + \theta)] \qquad \text{--- A7.25}$$

Substituting Eqn. A7.24 and A7.25 in Eqn. A7.21 gives:

$$i(k) = \frac{I_p}{2}\ [\{H_1(\omega_0) + jH_2(\omega_0)\}\ \text{EXPj}(\omega_0 kT_s + \theta) + \{H_1^{*}(\omega_0) + jH_2^{*}(\omega_0)\}\ \text{EXP}(-j(\omega_0 kT_s + \theta)] \qquad \text{--- A7.26}$$

Using Eqns. A7.9 and A7.12 we have:

$$H_1(\omega_0) = \left(B\ \text{EXP}(j\psi_1) + A\ \text{EXP}(-j\psi_1)\right)\ \text{EXP}(-j\omega_0 T_w/2) \qquad \text{--- A7.27}$$

$$H_2(\omega_0) = j\ \left(B\ \text{EXP}(j\psi_1) - A\ \text{EXP}(-j\psi_1)\right)\ \text{EXP}(-j\omega_0 T_w/2) \qquad \text{--- A7.28}$$

$$H_1^{*}(\omega_0) = \left(B\ \text{EXP}(-j\psi_1) + A\ \text{EXP}(j\psi_1)\right)\ \text{EXP}(j\omega_0 T_w/2) \qquad \text{--- A7.29}$$

$$H_2^*(\omega_0) = -j\ \left(B\ EXP(-j\psi_1) - A\ EXP(j\psi_1)\right)\ EXP(j\omega_0 T_w/2) \quad \text{--- A7.30}$$

In order to substitute Eqns. A7.27 to A7.30 in Eqn. A7.26, the following terms can be expressed as follows.

$$H_1(\omega_0) + jH_2(\omega_0) = 2A\ EXP(-j\psi_1)\ EXP(-j\omega_0 T_w/2) \quad \text{--- A7.31}$$

$$H_1^*(\omega_0) + jH_2^*(\omega_0) = 2B\ EXP(-j\psi_1)\ EXP(j\omega_0 T_w/2) \quad \text{--- A7.32}$$

Thus, Eqn. A7.26 can be expressed as follows.

$$i(k) = I_p\ EXP(-j\psi_1)\ [A\ EXPj\left(\omega_0(kT_s - T_w/2) + \theta\right) + B\ EXP-j\left(\omega_0(kT_s - T_w/2) + \theta\right)] \quad \text{--- A7.33}$$

Eqn. A7.33 can be expressed as follows.

$$i(k) = C_1\ EXP(-j\psi_1) \quad \text{--- A7.34}$$

where

$$C_1 = I_p\ [A\ EXPj\left(\omega_0(kT_s - T_w/2) + \theta\right) + B\ EXP-j\left(\omega_0(kT_s - T_w/2) + \theta\right)] \quad \text{--- A7.35}$$

Similarly, i(k-1) can be expressed as follows.

$$i(k-1) = C_2\ EXP(-j\psi_1) \quad \text{--- A7.36}$$

Using Eqns. A7.35 and A7.36, Eqn. A7.20 gives:

$$D(k) = Im\ \ C_1\ C_2^*\ EXP(-j\psi_1)\ EXP(j\psi_1) \quad \text{--- A7.37}$$

Eqn. A7.37 clearly shows that the determinant term is independent of the filter parameter ψ_1 as introduced in Eqns. A7.9 and A7.12.

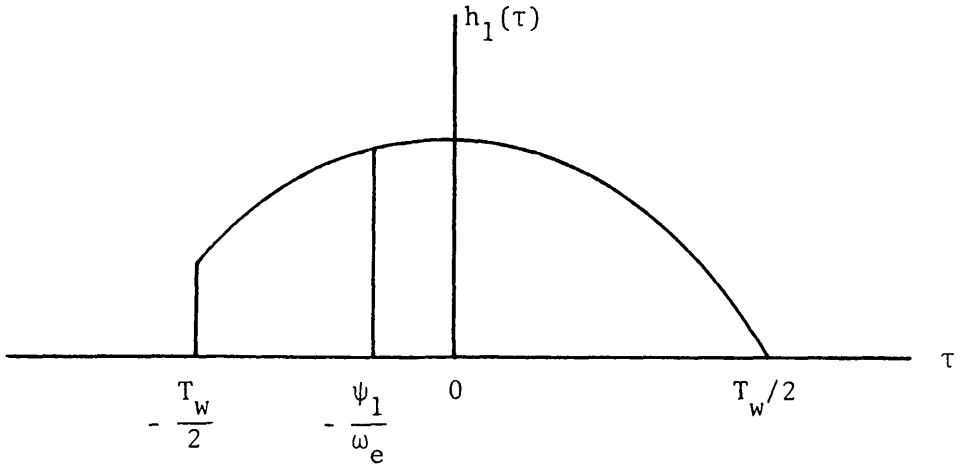


Fig. A7.1 : Cosine convolution filter impulse response

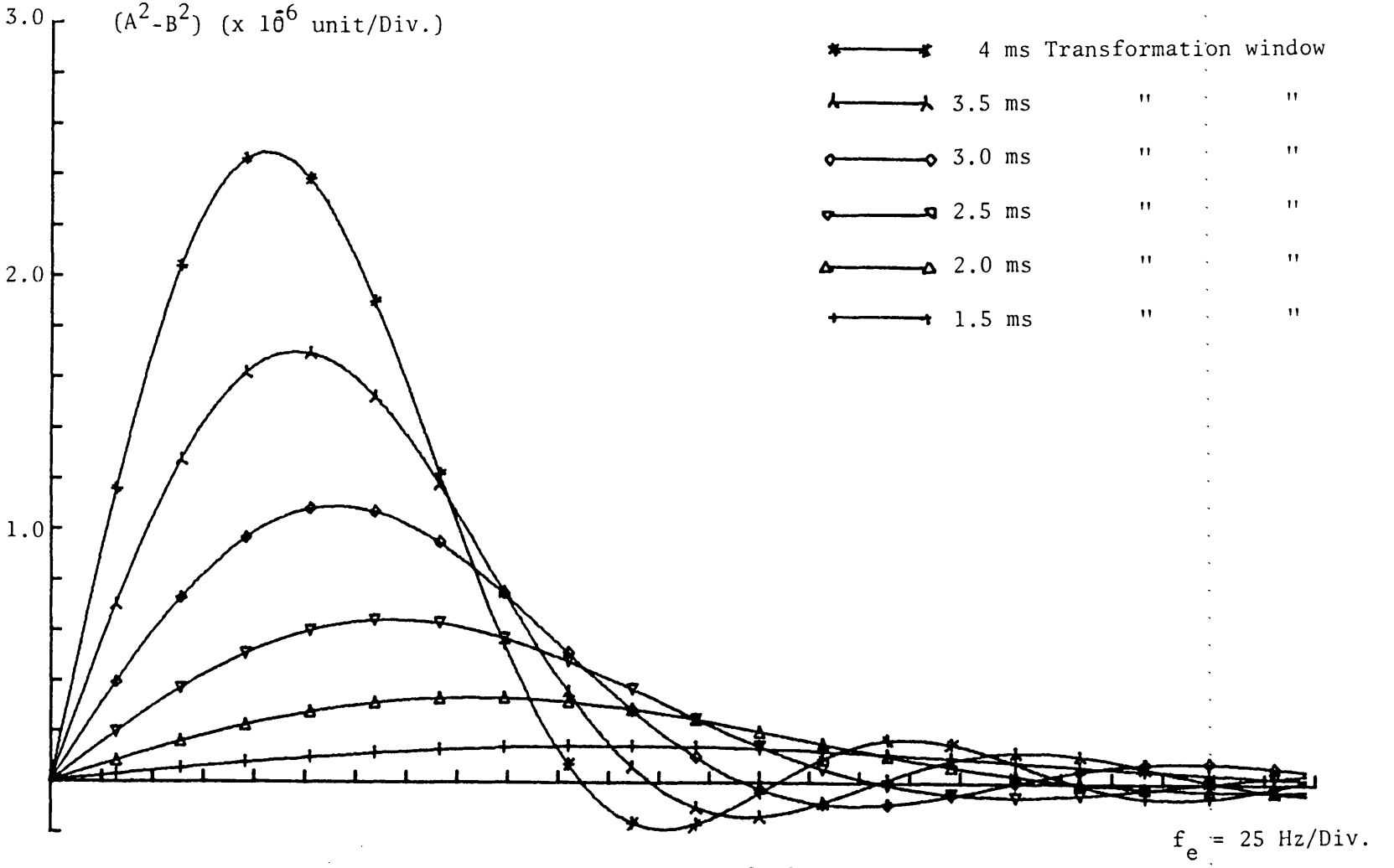


Fig. A7.2 : The magnitude of the determinant term (A^2-B^2) for various transformation windows against the extraction frequency

APPENDIX 8

FAULT DATA SCALING

Fig. 8.1 shows the relaying signals interface. For a 400 kV line, we have a (120% nominal phase voltage peak V_p) of:

$$V_p = \frac{1.2 \times 400000 \times 1.414}{(3)^{1/2}} \qquad \text{--- A8.1}$$

Internal to the relay, this is required to give a phase voltage signal Sv of 10 Volt, therefore:

$$K_v K_{vt} = Sv/V_p = 1/39191.836 \qquad \text{--- A8.2}$$

In order to achieve a greater accuracy, it is desirable that the current signal Si internal to the relay be nominally of the same magnitude as Sv for a fault at the relay reach, i.e.

$$Si = Sv \qquad \text{--- A8.3}$$

As described in Section 8.6.2, the sine and cosine convolution filters have different gains at 50 Hz. However, for a fault at the relay reach, the Fourier Transform components are set to have the same magnitude, since if the voltage and current sine components are scaled by the same factor (likewise the cosine components), the constraints of Eqns. 4.34 and 4.35 would not be in error. The relation between the phase voltage and the phase current is given by Eqn. A8.4:

$$I_p = V_p/Z\ell_1 \qquad \text{--- A8.4}$$

where $Z\ell_1$ is the p.p.s. impedance at the relay reach, therefore the current scaling factor can be written as:

$$K_c K_{ct} = Si/I_p = Z\ell_1 \, K_v K_{vt} \qquad \text{--- A8.5}$$

For a 128 km line, $Z\ell_1$ at the relay reach is 29.419 Ω, see Appendix 1, therefore $K_c K_{ct}$ is given by:

$$K_c K_{ct} = 1/1332.19 \qquad \text{--- A8.6}$$

thus, by scaling the simulated fault data by 39191.836 and 1332.19 for the phase voltage and current respectively, the current and voltage signals have the same magnitude internal to the relay for faults at 100% of the relay reach.

For phase-phase elements, the PTL scaling factors are as follows:

$$v_{ab}(t) = v_a(t) - v_b(t) = \left(\frac{K_c K_{ct}}{3^{1/2}} v_a(t) - \frac{K_v K_{vt}}{3^{1/2}} v_b(t) \right) \qquad \text{--- A8.7}$$

$$i_{ab}(t) = i_a(t) - i_b(t) = \left(\frac{K_c K_{ct}}{3^{1/2}} i_a(t) - \frac{K_v K_{vt}}{3^{1/2}} i_b(t) \right) \qquad \text{--- A8.8}$$

APPENDIX 9

LUMPED PARAMETER SINGLE PHASE MODEL

FOR COMPUTER PROGRAMMING

Consider the lumped parameter model shown in Fig. A9.1. The relation between the voltage and current is given by Eqn. A9.1 [25].

$$E \, SIN(\omega_0 t + \theta) = Ri(t) + L \, di(t)/dt \qquad \text{--- A9.1}$$

Assume the steady state current is(t) of the form given by Eqn. A9.2.

$$is(t) = A \, EXPj(\omega_0 t + \theta) + B \, EXP\text{-}j(\omega_0 t + \theta) \qquad \text{--- A9.2}$$

In order to find the steady state current, the coefficients A and B must be found. Using the sine function identity given by Eqn. A9.3.

$$SIN(X) = \frac{1}{2j} \left(EXP(jX) - EXP(-jX)\right) \qquad \text{--- A9.3}$$

and substituting from Eqn. A9.2 and Eqn. A9.1, Eqn. A9.4 is derived.

$$E/2j \, [EXPj(\omega_0 t + \theta) - EXP\text{-}j(\omega_0 t + \theta)] = R[A \, EXP \, j(\omega_0 t + \theta) + B \, EXP\text{-}j(\omega_0 t + \theta)]$$
$$+ L \, [jA\omega_0 \, EXPj(\omega_0 t + \theta) - jB\omega_0 \, EXP\text{-}j(\omega_0 t + \theta)] \qquad \text{--- A9.4}$$

Equating the coefficients in Eqn. A9.4 gives:

$$A = \frac{E}{2j(R + j\omega_0 L)} = \frac{E}{2jZ} \qquad \text{--- A9.5}$$

$$B = \frac{E}{2j(R - j\omega_0 L)} = \frac{E}{2jZ^*} \qquad \text{--- A9.6}$$

where $Z = R + j\omega_0 L = |Z|EXP(j\phi)$, $|Z|$ is the impedance magnitude given by:

$$|Z| = (R^2 + \omega_0{}^2 L^2)^{1/2} \qquad \text{--- A9.7}$$

and the impedance angle ϕ is given by:

$$\phi = \text{ARCTAN } (\omega_0 L/R) \qquad \text{--- A9.8}$$

The term Z^* is the impedance complex conjucate and $Z^* = |Z|\text{EXP}(-j\phi)$.

Substituting Eqns. A9.5 and A9.6 in Eqn. A9.2 gives:

$$is(t) = \frac{E}{2j}\left[\frac{\text{EXP } j(\omega_0 t + \theta)}{Z} - \frac{\text{EXP } -j(\omega_0 t + \theta)}{Z^*}\right] \qquad \text{--- A9.9}$$

Using the identity given by Eqn. A9.3 gives:

$$is(t) = \frac{E}{|Z|}\,\text{SIN}(\omega_0 t + \theta - \phi) \qquad \text{--- A9.10}$$

Combining the steady state current is(t) with the transient current component it(t) gives:

$$i(t) = is(t) + it(t) = \frac{E}{|Z|}\,\text{SIN}(\omega_0 t + \theta - \phi) + K\,\text{EXP}\,\frac{Rt}{L} \qquad \text{--- A9.11}$$

In order to determine the transient coefficient K, we set i(t) = 0 at t = 0, and obtain:

$$K = \frac{E}{|Z|}\,\text{SIN}(\theta - \phi) \qquad \text{--- A9.12}$$

Substituting Eqn. A9.12 in A9.11 gives:

$$i(t) = \frac{E}{|Z|}\,\text{SIN}(\omega_0 t + \theta - \phi) + \text{SIN}(\theta - \phi)\,\text{EXP}\,\frac{Rt}{L} \qquad \text{--- A9.13}$$

A9.1 LUMPED PARAMETER VOLTAGE AND CURRENT SIMULATION FOR 400 kV, 128 km LINE

A9.1.1 Pre-fault phase voltage and current

$$v_a(t) = V_p\,\text{SIN}(\omega_0 t + \theta) \qquad \text{--- A9.14}$$

$$I_a(t) = 0$$

where $V_p = \dfrac{400000 \times (2)^{1/2}}{3^{1/2}}$

A9.1.2 Post-fault phase voltage and current

$$v_a(t) = V_p \, SIN(\omega_0 t + \theta) \, Kv \qquad \text{--- A9.15}$$

$$I_a(t) = I_p \, SIN(\omega_0 t + \theta - \phi) - I_p \, SIN(\theta - \phi) \, EXP-(t/\tau) \qquad \text{--- A9.16}$$

where $Kv = \dfrac{Z_{s\ell}}{Z_{s\ell} + Z_s}$

$$I_p = \frac{V_p \, Kv}{Z_{s\ell}} = \frac{V_p}{Z_{s\ell} + Z_s}$$

$$\tau = \frac{L}{R} = 0.3183$$

$$\phi = ARCTAN \frac{X}{R} = ARCTAN \, \omega_0 \tau$$

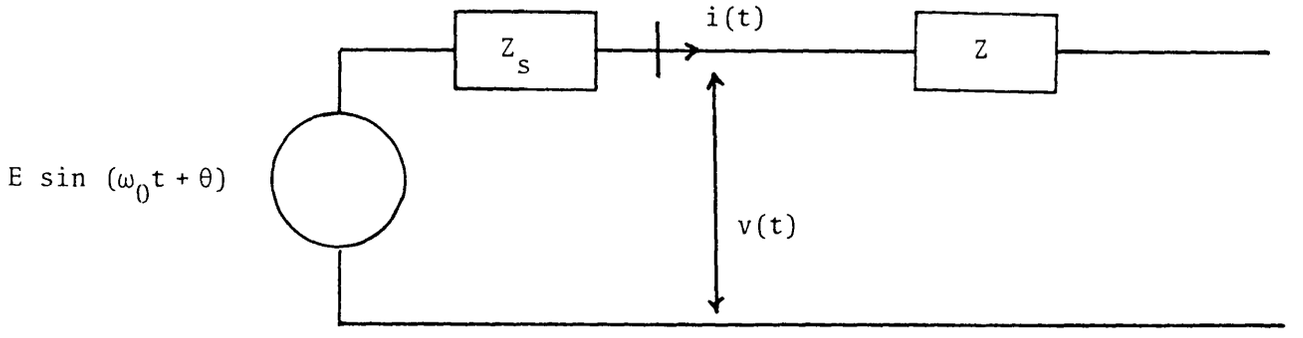


Fig. A9.1 : A lumped parameter circuit

APPENDIX 10

RESISTIVE FAULT EFFECT ON THE IMPEDANCE REACH

Consider a resistive faulted line shown in Fig. A10.1, and its equivalent circuit Fig. A10.2. From Fig. A10.2, the relaying voltage can be expressed as:

$$V_r = I1\ (\alpha Z\ell_1) + (I1 + I2)\ R_f \qquad \text{--- A10.1}$$

The measured p.p.s. impedance by the relay ($V_r/I1$), can be written as:

$$Z\ell_1(\text{meas}) = \alpha Z\ell_1 + R_f + (I2/I1)\ R_f \qquad \text{--- A10.2}$$

For a solid fault, $R_f = 0$ the impedance measured by the relay is proportional to $\alpha Z\ell_1$. However for resistive fault, there are two additional components, one proportional to the fault resistance and the second is proportional to the two sources fault current ratio.

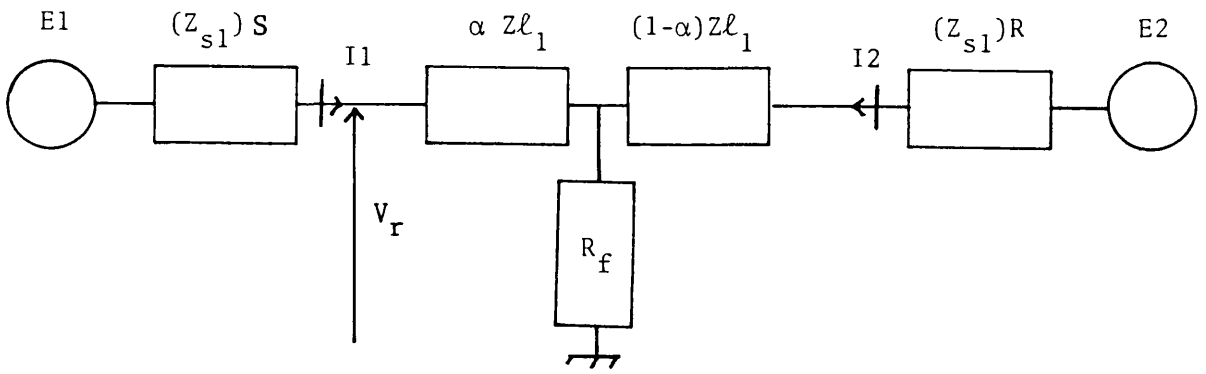


Fig. A10.1 : Resistive fault circuit representation

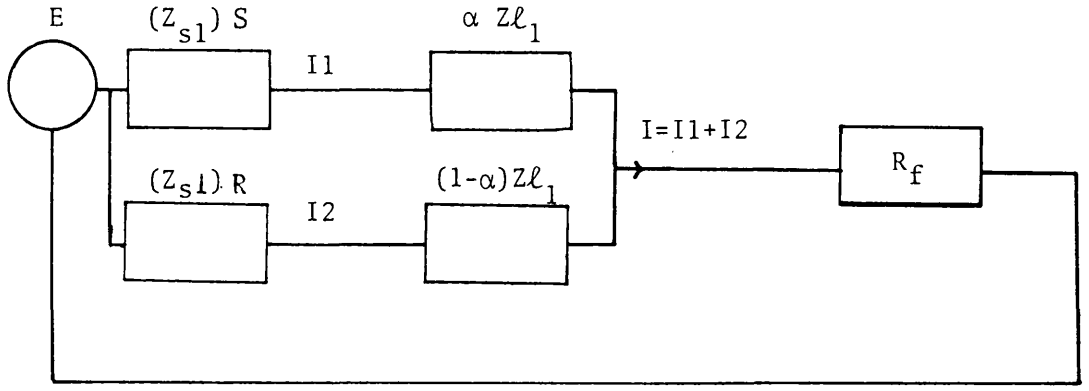


Fig. A10.2 : Resistive fault equivalent circuit

APPENDIX 11

DIGITAL DIFFERENCING PROCESS

Consider a crude differencer, which has a transfer function expressed in the form of Eqn. A11.1.

$$H(z) = 1 - z^{-1} \qquad \text{--- A11.1}$$

The differential term $i'(t)$ can be expressed in the discrete form of Eqn. A11.2.

$$i'(t) = \frac{i(k) - i(k-1)}{T_s} \qquad \text{--- A11.2}$$

In order to determine the differencing process frequency response, Eqn. A11.1 transforms to Eqn. A11.3.

$$H(j\omega) = 1 - \text{EXP}(-j\omega T_s) \qquad \text{--- A11.3}$$

Using the identity EXP -jX = COS X - j SIN X, Eqn. A11.3 can be expressed as,

$$H(j\omega) = (1 - \text{COS}\ \omega T_s) + j\ \text{SIN}\ \omega T_s \qquad \text{--- A11.4}$$

Thus the magnitude of the frequency response can be expressed as,

$$|H(j\omega)| = |2(1 - \text{COS}\ \omega T_s)|^{1/2} \qquad \text{--- A11.5}$$

Similarly, for an n-stage differencer, the magnitude of the frequency response can be expressed as,

$$|H(j\omega)| = |2(1 - \text{COS}\ n\omega T_s)|^{1/2} \qquad \text{--- A11.6}$$

where the differentiation term can be expressed in discrete form as,

$$\dot{i}(t) = \frac{i(k) - i(k-n)}{nT_s} \qquad \text{--- A11.7}$$

Fig. A11.1 shows the frequency response of a crude differencer and a 5-stage differencer (n = 5). For the crude differencer, the frequency response clearly shows that high frequency components are accentuated. Although the 5-stage differencer has a set of zeros in the frequency response, nevertheless frequency components between these zeros are accentuated. Therefore, the differencing noise must be filtered.

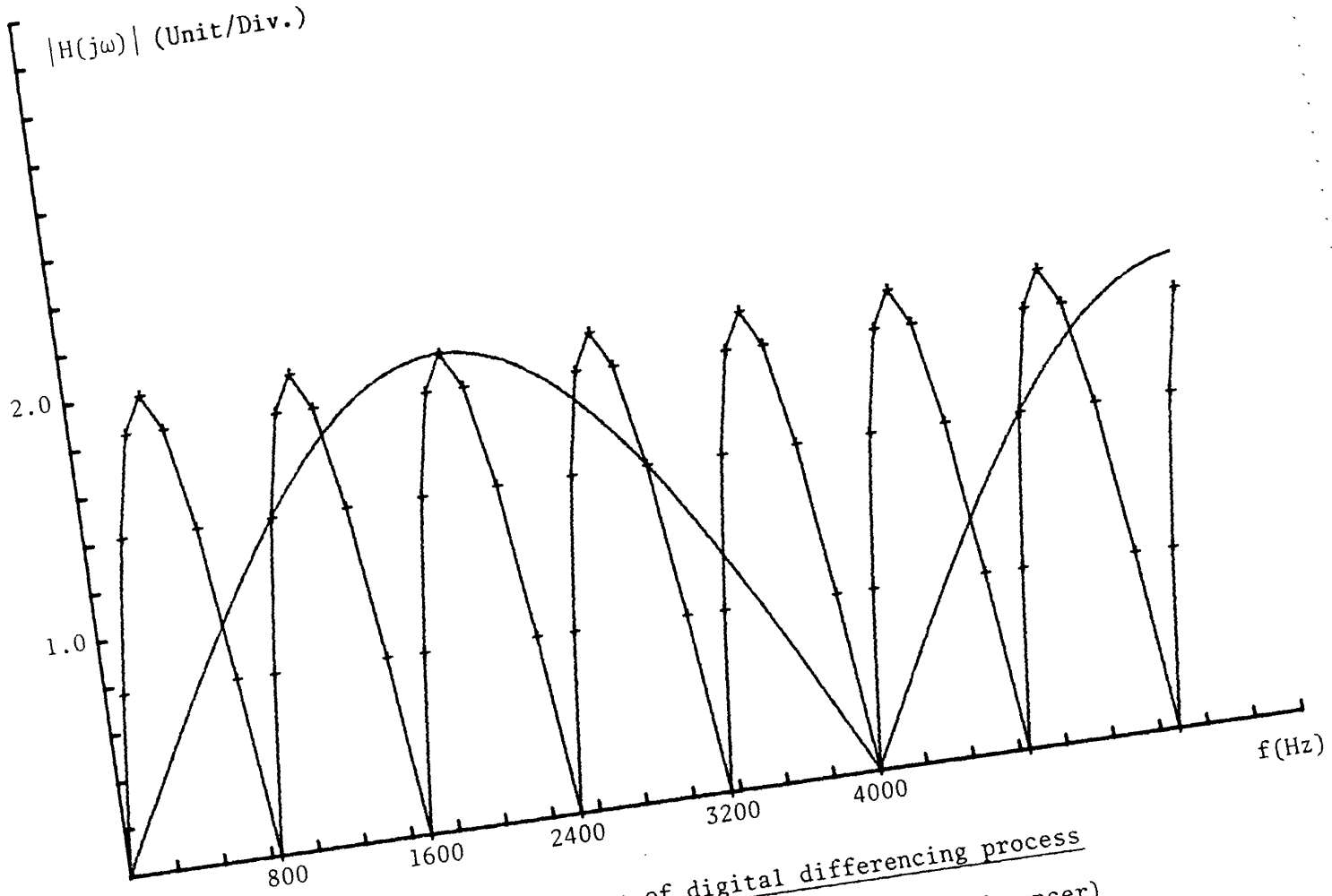


Fig. A11.1 : The frequency response of digital differencing process

—— one-stage differencer (crude differencer)

—×— 5-stage differencer

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